Evaluation Board Reference Manual

for EVB002 rev 0hb with G144A12 chips

Supported by arrayForth® Version 3

The GreenArrays EVB002 Evaluation Board is a versatile and powerful application development platform for the GA144-1.20 chips. Using arrayForth 3, the EVB002 may serve as a standalone development system with polyFORTH® running on the EVB002 directly, or may be used in conjunction with saneFORTH on x86 platforms. Its many configuration options facilitate intimate, interactive code development at all levels with one or two GA144 chips.

Please familiarize yourself with this information before using the Eval Board so that you will be aware of the many configuration options available to you.

In addition, please download and read the other relevant documentation such as the Programmers' Reference for the F18 computers (DB001), the G144A12 Chip Data Book (DB002), and the User's Manuals DB013 for arrayForth 3, DB005 and DB006 for polyFORTH, and other Application Notes as appropriate. The current editions of all GreenArrays documents, including this one, may be found on our website at http://www.greenarraychips.com .

It is always advisable to ensure that you are using the latest documents before starting work.

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1. Introduction

This is the primary reference manual for the EVB002 Evaluation Board. With two GreenArrays G144A12 chips, peripherals sufficient for a complete software and hardware development environment, and a large prototyping area, this highly configurable board is intended to serve both engineers and programmers well in evaluating our chips in all stages of application development.

Initially shipped with polyFORTH in flash, this board is ready for immediate software development using our arrayForth 3 tools. In addition, our Application Notes will use this board (as well as its predecessor, the EVB001) as their default platform so that our customers may make immediate use of the hardware and software solutions published in those exercises.

1.1 Relationship to EVB001

The EVB002 is upward compatible from EVB001 with several notable improvements.

- Several layout errors in the EVB001 are corrected. The activity LEDs associated with the FTDI USB Serial chips now work correctly. Unnecessarily large and therefore high voltage capacitors in the power supply have been replaced by smaller, 25V caps. The inverted hole pattern for the VGA connector has been corrected. Metal finish has been upgraded, silk screen cleaned up, and all vias that aren't actual test points are now solder masked.

- To facilitate use of polyFORTH running on the board itself as the primary development system for the EVB002, the SPI flash has been enlarged from 1 MB to 16 MB, the limit of conventional 24-bit SPI memory addressing, so that there is plenty of room for lots of code and data as well as backups and reconciliation copies. Unfortunately, this is not strictly upward compatible from the EVB001 in terms of software because the mode of multi-byte writing supported by the flash memories on the EVB001 is mutually exclusive with the mode supported by practically all SPI flash memories manufactured since then. Worse, although it is feasible to rework an EVB001 with the larger flashes despite the larger packages, there is also a circuit difference because the modern flashes do not uniformly support a reset signal on pin 7 and therefore the CE- signal coming from 705.3 on the GA144 must be pulled up.

- GreenArrays no longer supports the previous arrayForth tools based on colorForth. The final release (02b) of these tools, configured for EVB001, remains available on our website as does its documentation, and it is suitable for use on the EVB002 except that it does not correctly handle the new 16MB flash (see above). We have not done any further released development of colorForth since then, and we no longer provide free support of software based on colorForth. All new tools developed and supported by GreenArrays have been and will be based on polyFORTH for our chips and saneFORTH for Windows 32-bit API on x86 computers, as is the case with arrayForth 3 and with our new CAD system (GLOW).

- Experience has taught us that open drain level shifters are more practical for bidirectional use than are the push-pull versions on the EVB001. Half of these chips (U14, 15 and 16) are now open drain.

- The software defined Ethernet 10BaseT NIC has accumulated enough thousands of hours of reliable operation that we've replaced the relatively useless space occupied by four SMA connector hole patterns at the bottom of the prototyping area with the electrical interface for that NIC, including a dual op-amp to step up the transmit voltage swing, magnetics for the UTP transmission line interface, a 10 MHz crystal for transmit signal element timing and an RJ45 female connector. Four jumpers must be inserted between J21 and J48 to connect this circuitry with the host chip, and ≈5V must be supplied to J76 pin 2 or 4, for example from the raw input voltage supplied by USB or wall wart. polyFORTH as distributed includes support for some of the Internet Protocols. It is also possible to mount the E-NET piggyback board, made for EVB001, on this board.

- A reset/watchdog circuit is now available as a reset source for the Host chip.

1.2 Related Documents

This book describes an application of GreenArrays' chips, in particular the GA144. In the interest of avoiding needless and often confusing redundancy, it is designed to be used in combination with other documents.

The general characteristics and programming details for the F18A computers and I/O used in the GA144 are described in a separate document; please refer to DB001, *F18A Technology Reference*. The boot protocols supported by the chip are detailed in *Boot Protocols for GreenArrays Chips*. The configuration and electrical characteristics of the chip are documented in DB002, *G144A12 Chip Reference.* The software defined Ethernet NIC is described in AN007. Software User's Manuals DB013 for arrayForth 3, DB005 and DB006 for polyFORTH include instructions for installing and preparing these tools for use. The current editions of these, along with many other relevant documents and application notes as well as the current edition of this document, may be found on our website at http://www.greenarraychips.com ... see the complete list in "Index of Downloads". It is always advisable to ensure that you are using the latest documents before starting work.

Another important file in the same area of our website is *EVB002-Datasheets-r0h.zip* containing manufacturer's data sheets for those components (other than the G144A12) an advanced user of the board may need to know more about.

1.3 Status of Data Given

The data given herein are *Production,* reflecting boards starting with serial number 0201. If a section heading is highlighted in yellow, that heading and all text and subheadings subordinate to it are not yet converted/updated to reflect current hardware or software. The same is true of single text passages.

1.4 Documentation Conventions

1.4.1 Numbers

Numbers are written in decimal unless otherwise indicated. Hexadecimal values are indicated by explicitly writing “hex” or by preceding the number with the lowercase letter "x" which is syntax understood by all components of arrayForth 3.

1.4.2 Node coordinates

Each GreenArrays chip is a rectangular array of ***nodes,*** each of which is an F18 computer. By convention these arrays are represented as seen from the top of the silicon die, which is normally the top of the chip package, oriented such that pin 1 is in the upper left corner. Within the array, each node is identified by a three or four digit number denoting its Cartesian coordinates within the array as *yxx* or *yyxx* with the lower left corner node always being designated as node 000. Thus, for a GA144 chip whose computers are configured in an array of 18 columns and 8 rows, the numbers of the nodes in the lower right, upper left, and upper right corners are 017, 700, and 717 respectively.

When the programming context includes more than one chip, as it does in the case of the EVB002, node numbers generalize to the form ccyyxx where cc is zero-relative chip number.

1.4.3 Register names

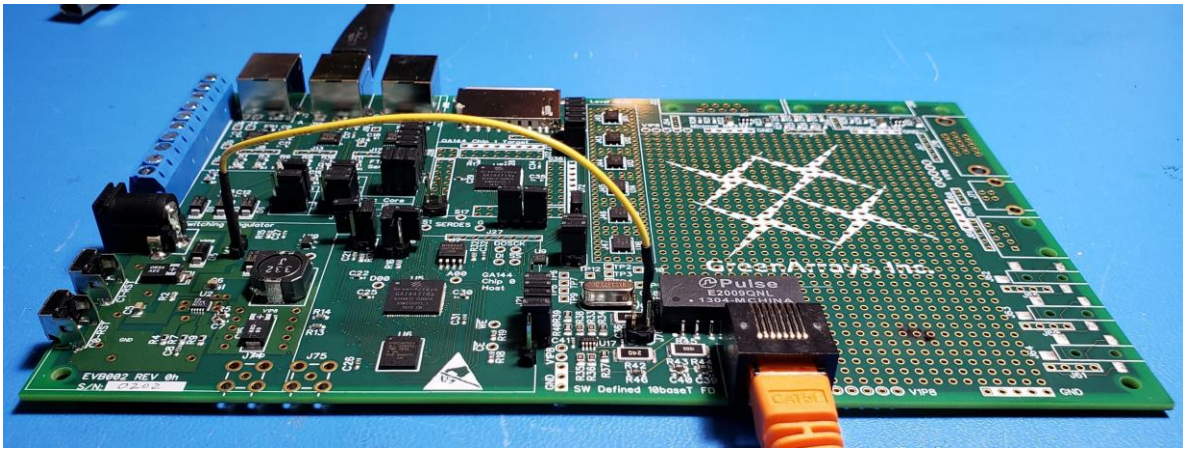
Register names in prose may be used with or without the word "register" and are usually shown in a bold font and capitalized where necessary to avoid ambiguity, such as for example the registers **T S R I A B** and **IO** or **io** .

1.4.4 Bit Numbering

Binary numbers are represented as a horizontal row of bits, numbered consecutively right to left in ascending significance with the least significant bit numbered zero. Thus bit *n* has the binary value 2^n. The notation P9 means bit 9 of register **P**, whose binary value is x200, and T17 means the sign (high order) bit of 18-bit register **T**.

2. Basic Architecture

The purpose of this board is to facilitate evaluation and application prototyping using GreenArrays chips. Because no single I/O complement would be suitable for all likely uses, this board has two GA144 chips: One (called "Host") configured with sufficient I/O for intensive software development, and the other (called "Target") with as little I/O committed as possible so that pure, dedicated applications may be prototyped.



2.1 Highlights

Three FTDI USB to serial chips provide high speed (960 kBaud) communications for interactive software development and general-purpose host communications.

An onboard switching regulator takes power from the USB connectors and/or a conventional "wall wart" power supply. Whichever of these is offering the highest voltage is used by the regulator.

A barrier strip provides for connection of bench power supplies. Each of the power buses of the two GA144 chips may selectively be run from external power in lieu of the onboard regulator, allowing you to run either chip from any desired V_{DD} voltage and also facilitating detailed current measurements.

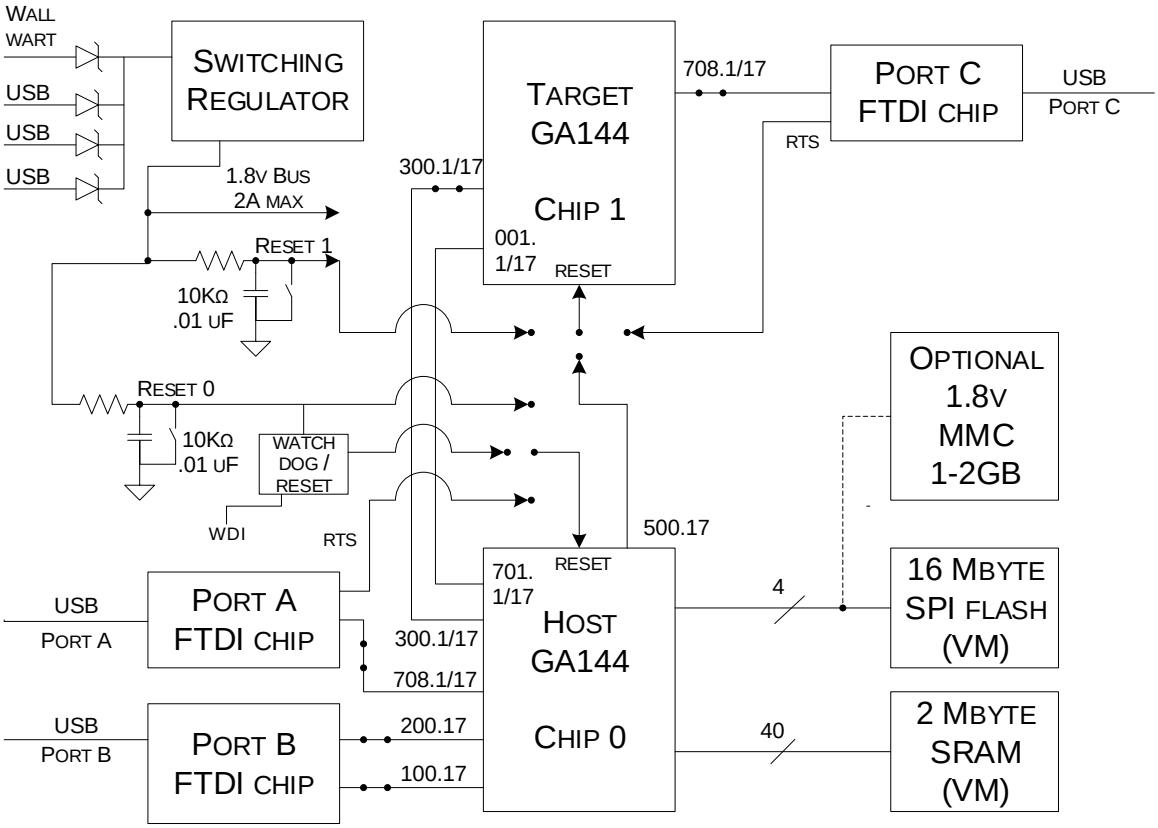
The Host chip is supplied with an SPI boot flash holding 16 MBytes of nonvolatile data, an external SRAM with 1 MWord (2 MBytes) of memory; and may optionally use a dual voltage MMC card such as the 2 Gigabyte unit we have selected for in-house use. These memory resources may be used in conjunction with Virtual Machines such as polyFORTH and eForth, or for direct use by your own F18 code.

The Target chip is committed to as few I/O connections as possible. The sources for its reset signal are fully configurable, and with the exception of a SERDES line connecting it with the Host chip, all of its connections (two 2-wire serial interfaces and the RESET line) may be disconnected so that the chip is fully isolated and thus all practical I/O is available for any desired use. The exception is a 1kΩ pull-up resistor on 705.17 to prevent SPI boot from putting signals on the other pins of node 705; this may be removed to minimize power use if signals on those pins aren't problematic. The chip may be programmed by the PC, or by the Host chip, in a variety of ways using arrayForth 3.

Ethernet physical interface circuitry and a watchdog/reset chip are available for use if desired. The board shown above was actively answering PINGs on the Internet when the photo was taken.

Roughly half the board is prototyping area, mainly populated with a grid of plated through holes on 0.1 inch centers. By soldering suitable headers to this grid, you can provide for expansion using various prototyping fixtures such as those made by SchmartBoard. The grid is intentionally large enough to support an 8- or 16-bit PC-104 socket. The periphery of the prototyping area is provided with hole patterns for many popular connectors, and there are six 8-bit bidirectional level shifters for interfacing with external circuits that may not run on 1.8v. In addition, one 1.8v 2-input OR and three NANDs are available for use in external circuitry.

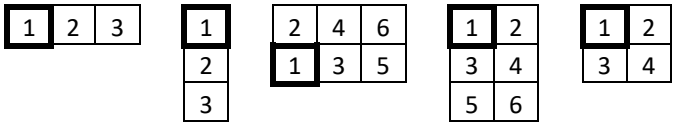
2.2 Simplified Block Diagram



As delivered, Host chip boots a Virtual Machine such as eForth or polyFORTH from flash and talks to terminal on RS232 port B. Ports A and C are available for IDE operations on Host and Target chips. Target may be fully isolated from Host with the exception of the SERDES connection. Other software options including other Virtual Machines besides eForth will be available for field upgrade.

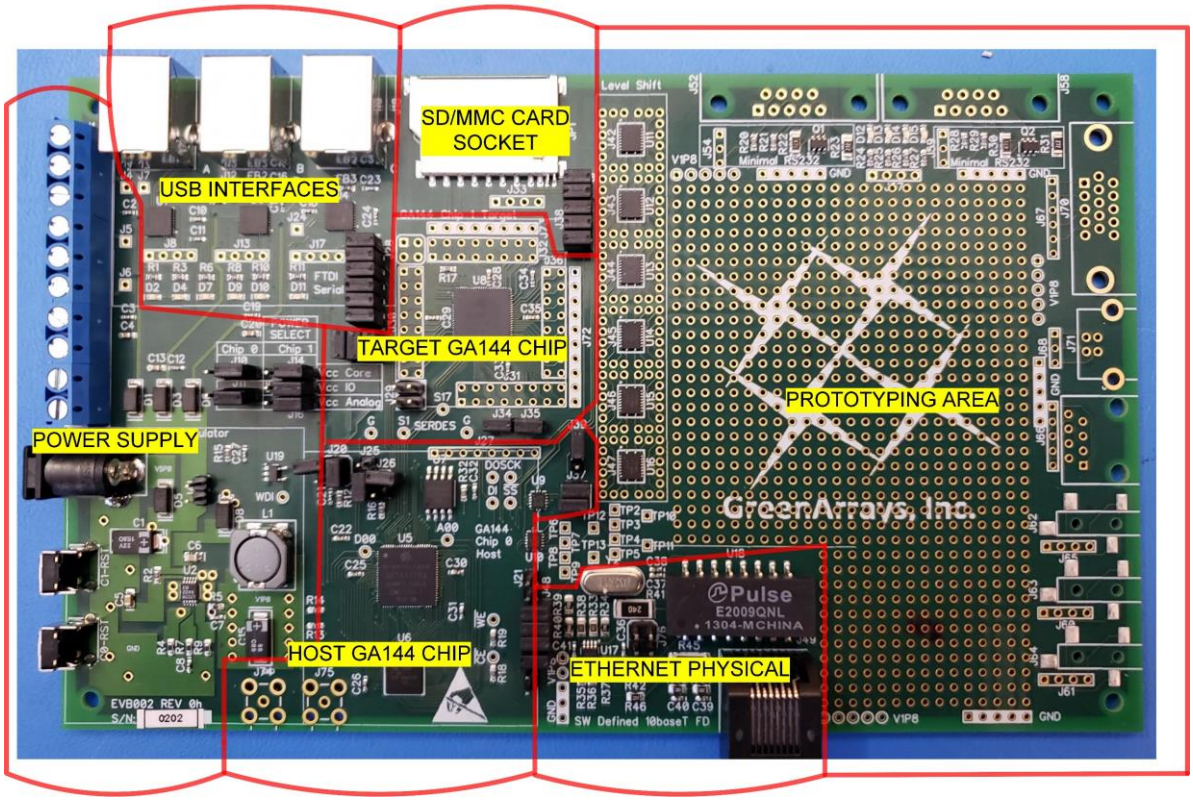
2.3 Header Orientation

For all single-*row* headers or hole patterns, pin 1 is at the left as viewed from the top side of the board with USB connectors in the upper left corner. For single *column* patterns, pin 1 is at the top. For headers with 2 pin short dimensions, pin 1 will be in the lower left corner for horizontally oriented patterns and in the upper left corner for vertical patterns. In the special case of 2x2 patterns, pin 1 is always in the upper left corner. The following diagrams illustrate these orientation conventions and pin numbering:



2.4 Board Floorplan

This overhead image of the evaluation board shows the spatial relationships among the subdivisions that are discussed in the following sections.



2.5 Software Support

This board is supported by several classes of software, listed below. Software options for GreenArrays chips and boards are continually being developed, and may be obtained from our website.

1. ***arrayForth 3*** is the tool for creation of software at all levels to run on our chips. Included are compilers, simulators, Interactive Development Environments (IDE), and boot stream generator. The arrayForth system is itself written in Forth, running on saneFORTH for PC and/or polyFORTH for the EVB002. Source code is maintained in ASCII.

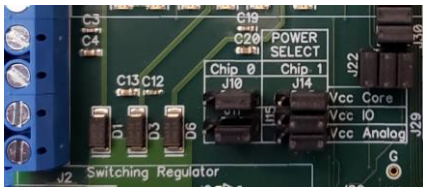
2. ***Virtual Machines*** running in clusters of F18 nodes support high level programming environments whose natures imply external memory resources. Examples are *polyForth* and *eFORTH* as well as special-purpose VMs such as the Snorkel and the Ethernet NIC. These environments may interact with microcode running in the rest of the chip, supervising or augmenting their high-performance activities.

3. ***Host platform applications***, such as enhanced terminal emulators, may be supplied with the virtual machines or other applications that use them.

4. ***Applications provided for this board*** include source code for arrayForth and/or for specific Virtual Machines, and often hardware configuration or modification instructions, as appropriate.

5. ***Third Party Tools*** have been created for our products. These are not supported by GreenArrays, but links are provided on our website.

3. Power Configuration



You must ensure there is enough power for the intended use of the board. Minimal USB (80% of 440 mW) is sufficient for eForth or polyFORTH and many typical projects, but power requirements can exceed 400 mW for $V_{DD}C$ (core power) if enough F18A computers are busy simultaneously, and likewise $V_{DD}I$ (I/O power) can be greater than this depending on what you connect to the chips. Several power sources are available in the upper left corner of the board.

3.1 Main 1.8v Bus

Primary 1.8v power is supplied by an onboard fixed voltage regulator fed by an optional "wall wart" (type N plug, positive center conductor, voltage *at the J2 connector* 3.6 to 19.5VDC with recommended minimum of 4.0V) and up to three USB connectors. Each source is diode protected from the others so whichever one is supplying the highest voltage will be the one that is used at any given time; these diodes have an internal drop of 200 to 300 mV. Each USB connector communicates with a USB host using an FTDI chip. The power available from each USB connection varies from a minimum of 100 mA at 4.4V to the maximum of 500 mA at 5V; the FTDI chips are configured to request permission to use the maximum to improve flexibility. An efficient (≈78%) switching regulator produces a maximum of 2A at 1.8V for the logic circuitry on the board. If this full rated power is needed, a "wall wart" capable of delivering 4.5 to 5 watts will be required (efficiency varies with voltage.)

The main 1.8v bus is used to power our side of the FTDI chips, the SPI flash, the Host chip's external SRAM, and the two logic chips used in SPI bus multiplexing. This bus is also the default source of $V_{DD}C$, $V_{DD}I$ and $V_{DD}A$ for the Host and Target chips. Finally it is available to power the SD/MMC socket, the level shifter chips, and is routed for easy availability in the prototyping area.

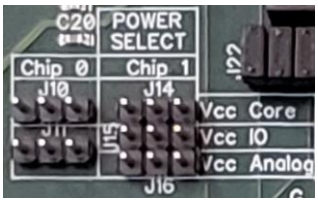
3.2 External DC Supplies

Barrier strip J1 provides for connecting up to five independent external power sources to this board, three of which are free for your use and wiring at J4, J5 and J6, while two have defined uses. Pin 1 may be used as an alternate source for any of the Target chip's V_{DD} buses. Pin 3 may be used as an alternate source for the Host chip's $V_{DD}C$ and/or its $V_{DD}I$ and $V_{DD}A$. This facilitates operating either or both of the chips at any desired supply voltage. It also provides for applications that require more than 2A of 1.8v.

3.3 Power Selection and Measurement

Five 3-pin headers allow selection of either the main 1.8v bus or an external supply as shown in this table:

Header	Chip	Bus	Pins 1-2 connected	Pins 2-3 connected
J10	Host	$V_{DD}C$	J1 pin 3	Main 1.8v Bus
J11		$V_{DD}I/A$		
J14	Target	$V_{DD}C$	J1 pin 1	
J15		$V_{DD}I$		
J16		$V_{DD}A$		



Current may be measured by inserting a shunt or other type ammeter across the desired pair of pins. Some combinations of current and shunt resistance will require use of an adjustable external power supply to give the desired voltage on the chip side of the shunt. *The jumpers provided are rated at 3A with max resistance of 20 mΩ.*

3.4 Other Available Voltages

An unregulated V_{CC} is input to the onboard switching regulator and may be used, with caution, from J41. In addition, each FTDI chip that is connected to a USB host can provide up to 50 mA of 3.3v, made available on J7, J12 and J19 for ports A, B and C respectively.

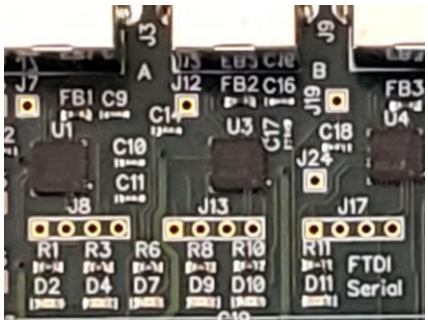
4. USB Interfaces

Three USB device interfaces provide for high speed communications with the GA144 chips. To a host computer each of these normally appears as an asynchronous serial (COM) port. Although each has a specific planned use on this board, their configuration is highly flexible.

4.1 Interface Devices

The devices provided are FT232R chips made by Future Technology Devices International, Ltd. (FTDI). As USB to serial UART devices, their USB side is powered by V_{CC} from the USB host while the side which talks to our chips is powered by the main 1.8v bus regulated on the board. Because the FTDI chips communicate with the GA144s directly using 1.8v CMOS, signals are crisp enough that each interface can run at an effective speed of 921,600 baud.

4.2 Jumpers and Connections



Transmit and receive lines are routed to the Host and Target GA144 chips as described in later sections. Request to Send (RTS) signals from ports A and C are available for chip reset purposes. RTS from port B is available at plated through hole J24.

Each FTDI chip is configured to drive transmit and receive activity LEDs D2, D4, D7, D9, D10 and D11 respectively. The remaining three configurable outputs, and the DTR signal, are available at hole patterns J8, J13 and J17 for ports A, B and C respectively. By default two of these outputs are configured with clock signals that may be used for time base purposes.

Each FTDI chip develops 3.3v for internal use. Plated through holes J7, J12 and J19 provide access to this supply from ports A, B and C respectively; up to 50 mA may be drawn from each of these for your circuitry if needed.

4.3 Flash Configuration

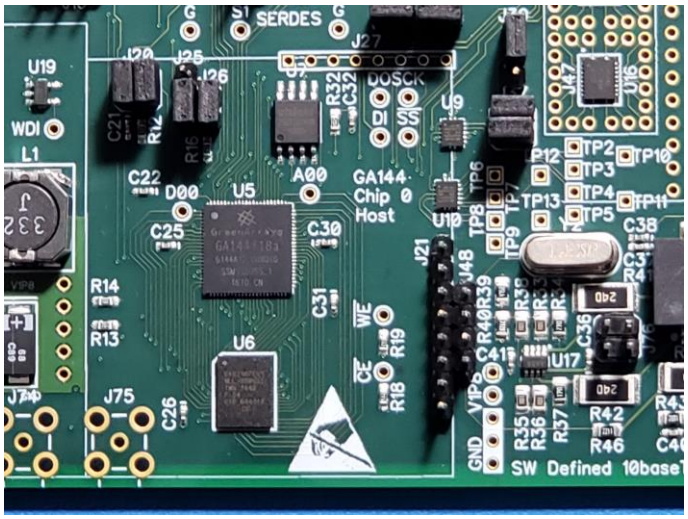
We configure the FTDI FT232RQ chips before shipping the boards by setting the polarities of TXD, RXD and RTS- lines correctly and by selecting our default outputs for the five CBUS lines as follows: CBUS0 and 1 are incoming and outgoing activity LED drivers respectively. CBUS2 and 3 are driven with clock frequencies generated by the FTDI chips. CBUS4 is also driven with the incoming activity signal as a work-around for one of the rev 0.1.1 board errata.

FTDI Signal	Signal Location			Definition
	Port A	Port B	Port C	
CBUS0-	(LED)	(LED)	(LED)	Driven low to indicate inbound ("TX") line activity.
CBUS1-	(LED)	(LED)	(LED)	Driven low to indicate outbound ("RX") line activity.
CBUS2-	J8.1	J13.1	J17.1	Clock output, 6 MHz.
CBUS3-	J8.2	J13.2	J17.2	Clock output, 48 MHz.
CBUS4-	J8.3	J13.3	J17.3	Driven low to indicate inbound ("TX") line activity.
DTR-	J8.4	J13.4	J17.4	Data terminal ready. Default state and polarity depend on driver software and configuration.

The FTDI chips are specially configured for their use on this board. Excellent documentation as well as configuration utilities and drivers are available from the manufacturer at http://www.ftdichip.com/. Template files are included in the software distribution. Please contact us before changing the configuration of your FTDI chips.

5. Host Chip

The Host chip, designated chip 0 on some of the design documentation, is by default configured as a development system including hardware and software support for a high-level language such as polyFORTH or eForth. The photo to the right shows the section of the board housing this powerful system including 144 F18 computers, two USB serial ports, 1 Megaword (2 MBytes) of external SRAM, 128 megabits (16 Mbytes) of bootable SPI flash, and optional provision for using a dual voltage MMC card as onboard mass storage. All connections make use of software defined I/O with minimal or no external circuitry. For example, U9 and U10 are included only to facilitate selection of multiple SPI devices.



Most host pins, other than those used to control SRAM, are available at jumper stakes or hole patterns such as J21 and J27. Several probe points are provided: WE-, CE-, A00 and D00 show SRAM timing; SS, SCK, DO and DI show signals at the SPI flash chip. S1 and S17 may be used, *with great care*, to probe the SERDES connection between Host and Target chips.

5.1 Reset Control

Host reset sources are an onboard RC with reset button; RTS signal from USB A; and U19, a MAX6823WUK+T 1.67V Reset / 1.6s watchdog circuit that in turn takes its reset signal from the RC and button. These are selectable:

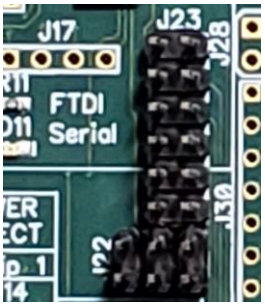
J20 pins	Reset Source
None	User provided inputs on pins 1 or 2
1-3	USB port A RTS signal
2-4	J25 selection
1-3 & 2-4	J25 selection or USB port A RTS

J25 pins	Source to J20 pin 4
1-2	Watchdog chip reset output
2-3	Host reset circuit / button

5.1.1 Reset/Watchdog Circuit

By default, the MAX circuit identified above is not connected. Because it includes a 1.6 second watchdog function, using it requires careful design of, almost certainly, flash boot code with boot enabled. There are various possible modes of operation but in general some node will need to be driving the WDI testpoint with a signal that does not stay in either state longer than 1.6 seconds. It is possible that our pins in high impedance look like a disconnected WDI, and if that is the case the watchdog *may* disable itself. It is less likely that weak pull-down will look that way. Careful design should be used to that the WDI signal meaningfully indicates that the application is still running satisfactorily so that we will only reset the chip if said application ceases doing what we want of it. Do not forget to consider how long it takes for the flash boot to complete, followed by convergence of the correct conditions for the first edge to be driven on the WDI line. You may wish to initialize **IO** low on the node doing the driving so the correct polarity for the first significant edge is established as high.

5.2 Serial Interfaces



USB port A is intended, by default, to be used for programming of the Host chip using the arrayForth Interactive Development Environment (IDE). Transmit and receive lines may be connected to async boot node 708 by insertion of jumpers in J23. Reset from port A may be connected as shown above. Port B is primarily intended to be used for a serial interface to the polyFORTH or eForth system; it too may be connected to nodes 100 and 200 by insertion of jumpers in J23. The mapping in J23 is as follows:

Signal	USB A			USB B			USB C		
	J23		Host	J23		Host	J23		Target
Rx to chip	1	2	708.17	5	6	200.17	9	10	708.17
Tx from chip	3	4	708.1	7	8	100.17	11	12	708.1

5.3 SPI Bus and Devices

Node 705 of the host chip is equipped with ROM capable of booting from an external flash memory using the 4-wire SPI interface. Using jumper options, node 705 may be configured to boot from the onboard flash chip. It may also be configured to selectively use other SPI devices under control of node 600 and/or external logic you provide. One option that is explicitly supported is selection of either the SPI flash or a 1.8v MMC card in the SD card socket provided with the board, under program control. Jumpers may also be used to completely disconnect node 705 from any of these things so its four pins are free for other application use.

5.3.1 SPI Flash and Booting

Jumper block J26 (NO BOOT) disables SPI flash chip booting when inserted. New flash chips do not have reset signals so those EVB001 options have been removed.

Evaluation boards are shipped with a bootable polyFORTH high-level virtual machine in flash. New software is initially loaded into flash using the arrayForth IDE; the procedure for doing this requires use of J26. For other uses of the flash by software packages such as polyFORTH, and for software installation procedures, see the documentation for each software package. For low-level application use, see arrayForth source code and application notes.

5.3.2 MMC Card Mass Storage

The SD card socket also accepts MMC cards, and because dual voltage MMC cards support 1.8v VDD and signaling logic levels, such cards may be directly controlled by the GA144. polyFORTH will in the future make use of such an MMC card as additional mass storage, and the board's jumpers are set by default to enable this. The MMC card may be used for backup, data logging, and transport of code or data between evaluation boards or other computers.

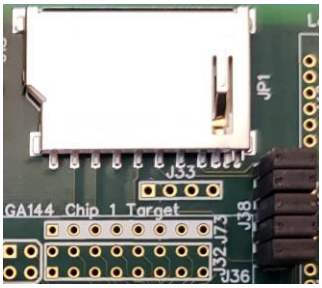
5.3.3 Enabling MMC Card Selection

Two jumper blocks configure simple external circuitry for selecting between multiple SPI devices on the 4-wire bus controlled by node 705. The standard configurations are as follow:

J39	J37	
1	1	2
2	3	4
3		

J39 pins	J37 pins	Configuration
2-3	1-2, 3-4	SPI Flash is always selected. Node 600 unused.
1-2	1-2, 3-4	Node 600 selects SPI flash when its pin is low (reset condition), or MMC card when the pin is high.

5.3.4 Connecting MMC Power and Signals to SD Socket



The selection logic described in section 5.3.3 drives signals that terminate in J40 near the SD card socket, along with 1.8v for V_{DD} on MMC cards. To configure the SD socket to use these signals and power a dual voltage MMC card, install five jumpers between each pin of J40 and the corresponding pin of J38.

5.4 SRAM

The external SRAM may be used with the virtual machines supporting high level languages, in which SRAM control software is inherently present, or it may be used directly by F18 applications. In the latter case, one option is to employ the SRAM control cluster (four nodes) supplied with arrayForth. Alternatively you may write your own. No optioning nor interface circuitry is needed; probe points are provided to facilitate I/O software development.

5.5 Connections to Target

Host SERDES node 701 is hardwired to Target node 001 with probe points. This connection may be used for programming or otherwise communicating with the Target, to evaluate the SERDES, and to explore and develop protocols.

Host node 500 drives a signal that connects to J22 pin 1 as one source of reset signal for the Target chip.

Host node 300 may be connected to Target node 300 using J34 and J35; this allows the Host to boot the Target using 2-wire synchronous protocol.

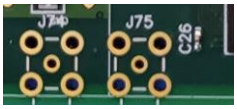
5.6 Summary of Host Pin Usage

Although many Host pins are committed to SRAM control, a good number remain available for application use.

5.6.1 Committed by Layout

All 40 pins of nodes 7, 8 and 9 are committed to SRAM control. Only four of these lines are available for probing. SERDES lines from node 701 are committed to Target communication.

5.6.2 Uncommitted



All ten Analog I/O pins are uncommitted, as are the GPIO pins of nodes 217, 317, 417, 517 and 715. These 15 pins are available on hole patterns J21 and J27.

Node 001.1 and .17 (SERDES data and clock) are available at SMA patterns J74 and J75 respectively.

5.6.3 Conditionally Available

Nodes 100 and 200 are committed only if polyFORTH or eForth is used; otherwise their GPIO pins are available. *All of the pins in this section are accessible at plated through holes or at jumper blocks.*

Node 300 has two GPIO pins which are available unless you require them for Target communication.

Node 500 has one GPIO pin that's available unless you need to use it for Target reset.

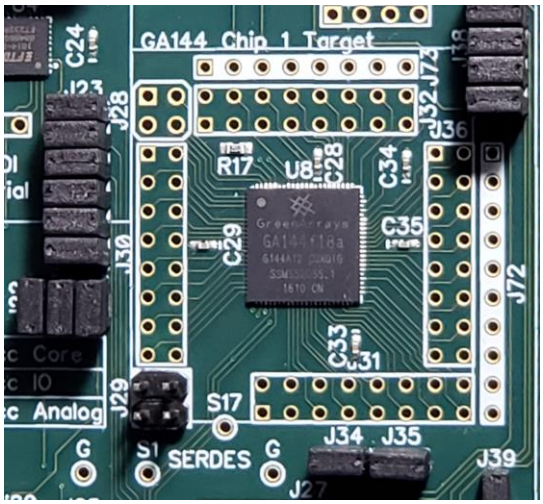
Node 600 has one GPIO pin that's available if you are not using the MMC card option.

Node 705 has four GPIO pins that are committed for SPI bus control, but if that is not needed the SPI chips can be disabled and all four pins are available. (Pin 17 must still be pulled high if you wish to prevent boot validity check when the chip is reset.)

Node 708 is normally used for arrayForth IDE but if not required these are available for asynchronous boot or any other desired use.

Four of the lines on J21 are committed when the software defined 10baseT NIC is being used.

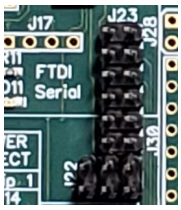
6. Target Chip



The Target chip, designated chip 1 on some of the design documentation, is configured in such a way that it may be booted and debugged, but otherwise all of its pins are available for your application. One possible use is as an I/O or computational expander for the Host chip. However the key reason for providing the Target chip on this evaluation board is to address your need to prototype a full application for a dedicated GreenArrays chip without having to lay out a board or disconnect a great deal of evaluation circuitry.

All but seven of the Target I/O pins are completely uncommitted, and are available in hole patterns J30, J31, J32 and J36 as shown in the picture at right. Of those seven, all but two may be disconnected with jumpers to isolate the Target chip for use in a dedicated application prototype.

6.1 Reset Control



Target reset is configured using J22 to the left of the chip. The three pins on the top edge of the header (2, 4 and 6) are connected in parallel to the RESET- pin of the Target chip. The other three pins are connected with reset sources that may be combined as a summing point. Pin 1 is connected to Host chip node 500; pin 3 is connected to USB port C RTS- line (low when RS232 signal would be low); and pin5 is connected to the power-on RC and pushbutton reset circuit for the Target chip.

J22		
2	4	6
1	3	5

6.2 Serial Interface

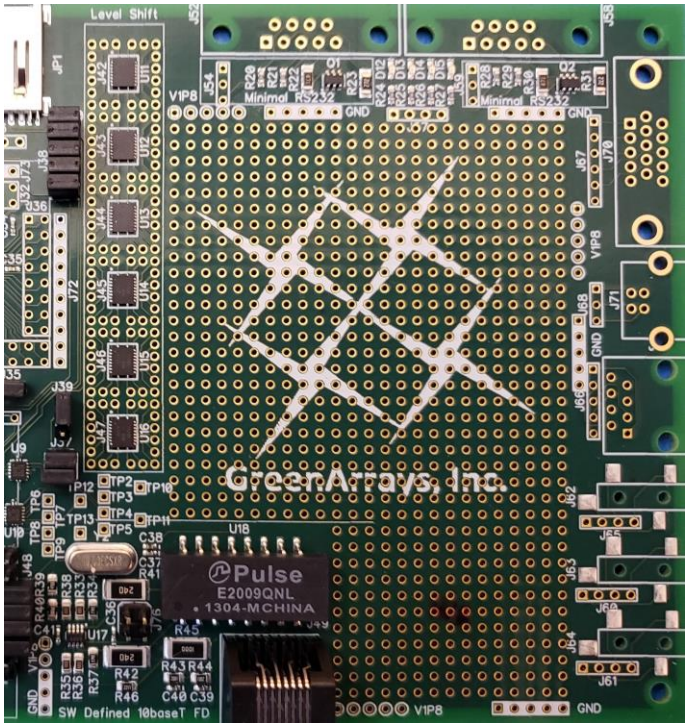
USB port C is available to be used for programming the Target chip using the arrayForth IDE. Transmit and receive lines may be connected to async boot node 708 by insertion of jumpers 9-10 and 11-12 of J23 located above the J22 reset control jumper, as shown earlier in section 5.2.

6.3 Host Chip Communications

As noted earlier, Host SERDES node 701 is hardwired to target node 001 with probe points as shown to the right.

Host node 300 may be connected with Target node 300 for booting or other communications. This is enabled by inserting jumpers J34 and J35 to the right of the SERDES probe points.

7. Prototyping Area



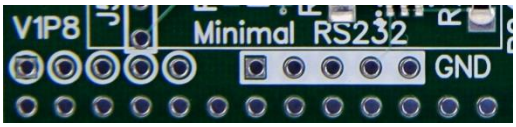
Roughly half of the evaluation board's area is available for your use in building any desired circuitry. We have made this as flexible as feasible for a broad range of projects. The area is covered with patterns of plated through holes to which you may solder components, connectors, headers and so on as necessary. On the grounds that it is simpler and easier to solder multi-pin devices onto a board than it is to remove such devices when they are in the way, we supply an assortment of connectors and headers in a separate bag for your use.

GreenArrays uses its evaluation boards as primary platforms for design exercises that will be published on our website. The resulting Application Notes suggest ways to make good use of this area.

7.1 Plated-through Hole Grid

The large grid of plated through holes, on 0.1" centers, gives almost unlimited flexibility in breadboarding your circuits. The area is compatible with many common technologies that may be used to attach components, interfaces, or expand the area further by soldering 0.1" headers to the board in suitable patterns. These options will be expanded upon later.

7.2 Power, Ground and Signals



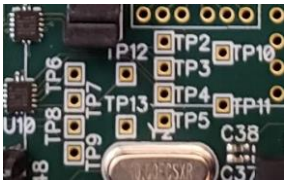
Hole patterns carrying the main 1.8v bus and common ground are available surrounding the prototyping area. Other supply voltages such as 3.3v from the FTDI chips or user supplied voltages from the J1 barrier strip must be hand wired, as must any other signals such as those from GA144 pins.

7.3 Convenience Circuits

For interfacing to devices with signal voltages other than the 1.8v native to the GA144, there are six 8-bit bidirectional level shifter chips in the prototyping area. These are Texas Instruments TXB0108 and TXS0108E devices in RGY packages and for maximum flexibility none of their pins are connected except ground (pin 11 and die attach paddle.) You may use each of these chips to interface between 1.2 to 3.6v on the A port and 1.65 to 5.5v on the B port by connecting suitable supply voltages to each of the chip's two V_{CC} pins.

In addition, there are four uncommitted 2-input, 1.8v CMOS logic gates available for your use. These are located between the Host chip and the hole grid of the prototyping area. The table below identifies the connections and gate types.

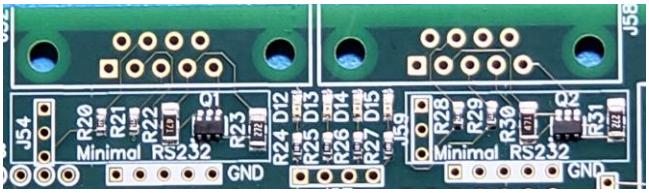
Inputs		Output	Gate Type
TP4	TP5	TP11	2-input NAND
TP6	TP7	TP12	
TP8	TP9	TP13	
TP2	TP3	TP10	2-input OR



7.4 Optional Connector Hole Patterns

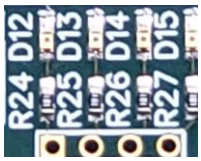
Unpopulated hole patterns are provided along the edges of the prototyping area for various connectors. Some connectors are supplied with the evaluation board so that you may solder in any that you require.

7.4.1 DB9 Connectors



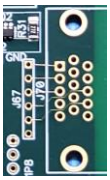
To interface with RS-232 devices, there are two female DB9 patterns. For your convenience, these are equipped with minimalist RS232 interfaces that may be used with our chips: Data receive and RTS signals are simply connected to GA144 pins through current limiting resistors, while data transmit is done with a pair of inverting N transistors powered by the Data Terminal Ready (DTR) line from the RS232 device. If these circuits don't do the trick, the components may be de-soldered and direct connection made to the DB9 pins. Pins 1 of J54 and J59 are received data going to the GA144, pins 2 are transmit from the GA144, and pins 3 are incoming RTS. The inactive state of each of these RS232 lines is low.

7.4.2 General-Purpose LEDs



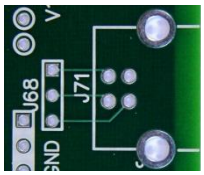
Located between the two DB9 patterns are four general-purpose LEDs, which may be turned on by supplying them with 1.8 volts on the geometrically corresponding pin of the adjacent pattern J57.

7.4.3 VGA Connector



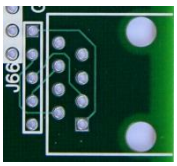
A pattern for a female 15-pin D shell provides the means for driving a VGA display directly from the GA144. Terminating resistor networks must be added if the device requires them.

7.4.4 USB Connector



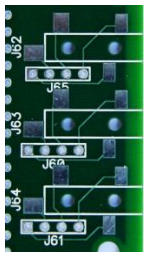
To facilitate development of USB device hardware and software, provision is made for attaching a USB type B receptacle to the prototyping area. Some interface circuitry will probably be needed.

7.4.5 RJ48 Connector



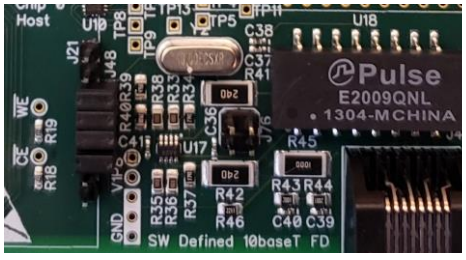
For development of 10baseT and perhaps other Ethernet interfaces, a pattern is provided for an RJ48 receptacle. Like USB, we expect that some minimal interface circuitry will be required as well.

7.4.6 Audio Connectors



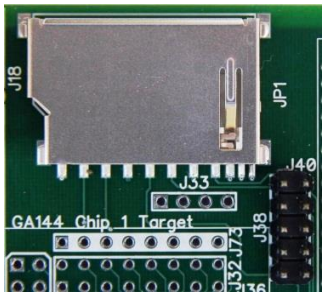
For analog audio input/output development, up to three 3.5mm stereo TRS receptacles may be soldered to patterns provided on the prototyping area.

7.4.7 Ethernet Physical Interface Circuitry



Minimal circuitry to interface the host chip directly to full duplex 10baseT Ethernet occupies one corner of the prototyping area. It may be used by the ATHENA TCP/IP package, distributed as part of polyFORTH. To use this circuitry, four jumpers must be inserted between the four physically adjacent pin pairs of J21 and J48, and a source of approximately 5V must be supplied to pins 2 or 4 of J76. If the board is being powered by USB or a 5V wall wart, 5V will be available on either pin of J41. This TCP/IP package is documented in DB008 and the NIC is documented in AN007.

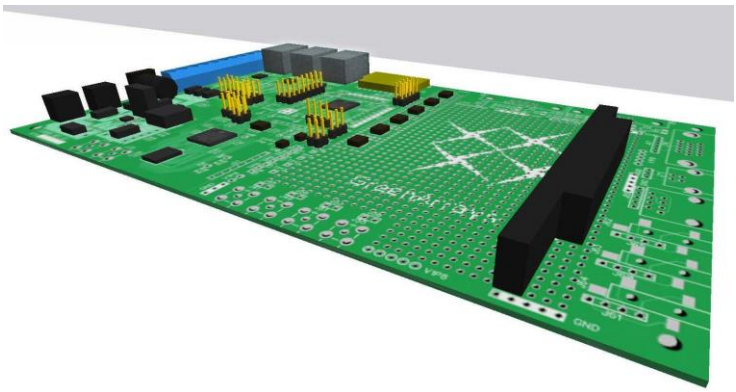
7.5 Optional use of SD socket



Although software being prepared for the evaluation board will be capable of taking advantage of a dual voltage MMC card for various purposes, the board layout is versatile enough to allow for development of code to access 3.3v SD cards as well. To take advantage of this capability, you must arrange to supply the SD socket with 3.3v power and construct the circuitry needed to communicate with it using 3.3v logic signals. All nine pins are available at the socket on J33 and J38, including two handshake lines, V_{DD} , all four data lines, card-present and write-protect signals.

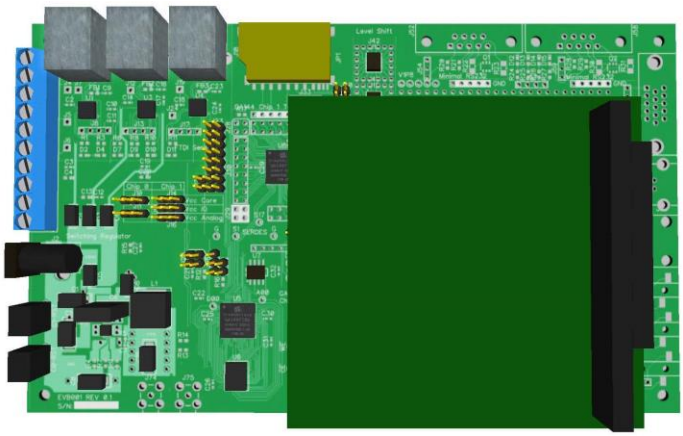
7.6 Expanding the Prototyping Area

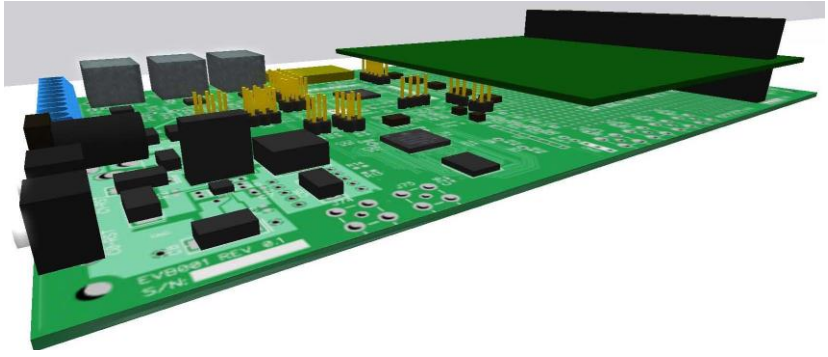
As suggested above, the grid of holes on 0.1" centers facilitates the installation of female headers into which various expansion devices may be plugged.



Schmartboard™ Products include small boards which can connect various surface mount parts to our prototyping area using 0.1" headers. This is considerably simpler and more likely to succeed than is "dead bugging" SMT components.

As another example, by soldering double row female headers appropriately in the prototyping area, PC-104 boards may be connected to the evaluation board. For example, see WinSystems® Products which include prototyping boards that could simply enlarge the prototyping area, or peripheral boards that could be used with level shifters. Here are two views of simulated 16-bit PC-104 connector and PC-104 board:





8. Physical Documentation

This section includes signal tables, schematics and PCB layout artwork.

8.1 Bill of Materials

RefDes	Value	Pattern	Qty	Manufacturer	Supplier	Sup Part No.
C1	22uf-25V	CAP TQC	1	Panasonic	Digi-Key	P16517CT-ND
C2, C3, C11, C12, C14, C17, C18, C19, C22, C24, C25, C26, C28, C29, C30, C31, C32, C33, C34, C35	0.1uF	CAP_0402	20	ATC American Tech Ceramics	Digi-Key	1284-1591-2-ND
C4, C13, C20	4.7uf	CAP_0603	3	Samsung	Digi-Key	1276-1907-2-ND
C5	0.22uF 25v	CAP_0805	1	Samsung	Digi-Key	1276-6477-2-ND
C6	0.47uF 25v	CAP_0805	1	Samsung	Digi-Key	1276-6480-2-ND
C7	470pF 5v	CAP_0402	1	Yageo	Digi-Key	311-3810-2-ND
C8	330pF 25v	CAP0402	1	KEMET	Digi-Key	399-15320-1-ND
C9, C10, C16, C21, C23, C27	10nF	CAP_0402	6	AVX	Digi-Key	478-1114-2-ND
C15	68uF 16V	CAP TQC	1	Panasonic	Digi-Key	P16218CT-ND
D1, D3, D5, D6, D8		Diode 403D0-2	5	ON SEMI	Digi-Key	MBRA340T3GOSCT-ND
D2, D4, D7, D9, D10, D11, D12, D13, D14, D15		CC0603	10	Dialight	Newark	75R0573
FB1, FB2, FB3		CR0603	3	Murata	Digi-Key	490-5247-1-ND
J1		TERMBLK10	1	On Shore	Digi-Key	ED2616-ND
J2		PJ-002B_CON	1	CUI Inc	Digi-Key	CP-002BH-ND
J3, J9, J18		USB-B	3	Adam Tech	Digi-Key	2057-USB-B-S-RA-ND
J10, J11, J14, J15, J16, J25, J39		CON_SIM	7	GA Break Up	GA	
J20, J29, J37		HEADER_2X2	3	GA Break Up	GA	
J22		HDR_2X3	1	GA Break Up	GA	
J23		HDR_2X6	1	GA Break Up	GA	
J26, J34, J35	No Boot	HEADER_1X2	3	GA Break Up	GA	
J38+J40 assemble as one		HEADER_2X5	1	GA Break Up	GA	
JP1		SD Short Card Conn	1	GCT	Newark	69R4862
K1, K2	C1-RST	Switch_PB	2	Panasonic	Digi-Key	P10877S-ND
L1	3.3uH	Inductor 3.3uh	1	COILCRAFT	Coilcraft	MSS1048-332NLC
Q1, Q2	Dual 50v N-FET	SOT-26	2	Diodes, Inc.	Digi-Key	DMN5L06DMKDICT-ND
R1, R3, R6, R8, R10, R11, R24, R25, R26, R27	180	RES_0603	10	Yangeo	Digi-Key	311-180GRTR-ND
R2	15K 10%	RES_0603	1	Panasonic	Digi-Key	P15KGTR-ND
R4	100K	RES_0603	1	Panasonic	Digi-Key	P100KHTR-ND
R5	127K 1%	RES_0603	1	Panasonic	Digi-Key	P127KHTR-ND
R7	18.2K 10%	RES_0603	1	Panasonic	Digi-Key	P18.2KHTR-ND
R9	68.1K 10%	RES_0603	1	Panasonic	Digi-Key	P68.1KHTR-ND
R12, R15	10K	RES_0603	2	Panasonic	Digi-Key	P10KGTR-ND
R13, R14, R16, R17, R32	1K	RES_0603	5	Panasonic	Digi-Key	P1.0KGTR-ND
R18, R19, R20, R21, R28, R29	5.1K	RES_0603	6	Panasonic	Digi-Key	P5.1KGTR-ND
R22, R30	470	RES_1206	2	Rohm	Digi-Key	RHM470ICT-ND
R23, R31	2.7K	RES_1206	2	Stackpole	Digi-Key	RMCF1206JT2K70CT-ND
U1, U3, U4	USB Serial	PQFN-32R/5x5x0.5	3	FTDI	Digi-Key	768-1008-1-ND
U2	Regulator	MSOP-10	1	Linear Technol	Arrow	LT3480EMSE#PBF
U5, U8	Multicomputer	QFN-88	2	GreenArrays	GA	G144A12
U6	SRAM	FBGA_48/6x8	1	Cypress	Mouser	727-C167EV18LL55BVXI
U7	SPI Flash	SOIC-8/209mil	1	Winbond	Digi-Key	W25Q128FWSIG-ND
U9	Quad OR	RQFN-14/2.5x3x0.5	1	Nexperia	Digi-Key	1727-3497-1-ND
U10	Quad NAND	RQFN-14/2.5x3x0.5	1	Nexperia	Digi-Key	1727-6947-1-ND
U11, U12, U13	Octal Levelshift	QFN-20_paste	3	TI	Newark	86W6392
U14, U15, U16	Octal Levelshift	QFN-20_paste	3	TI	Mouser	
U19	Reset/Watchdog	SOT23-5	1	Maxim	Digi-Key	**MAX6823WUK+T-ND**
Ether Only:						
C36, C37, C38, C39, C40, C41	0.1uF	CAP_0402	6	ATC	Digi-Key	1284-1591-2-ND
J21		CON_SIM	1	GA Break Up		
J41	**V5+**	HEADER_1X2	1	GA Break Up	Digi-Key	
J48		CON4	1	GA Break Up	Digi-Key	
J49		Ethernet	1	TE - AMP	Digi-Key	A31442-ND
J76		HEADER_2X2	1	GA Break Up	Digi-Key	
R33, R35, R36, R38	1K	RES_0805	4	Rohm	Digi-Key	RHM1.00KAECT-ND
R34	2.74k	RES_0805	1	Stackpole	Digi-Key	RMCF0805FT2K74TR-ND
R37	1.74k	RES_0805	1	Yageo	Digi-Key	311-1.74KCRTR-ND
R39	475	RES_0805	1	Stackpole	Digi-Key	RNCP0805FTD475RTR-ND
R40	392	RES_0805	1	Stackpole	Digi-Key	RMCF0805FT392RTR-ND
R41, R42	24	RES_2512	2	Stackpole	Digi-Key	RMCF2512JT24R0CT-ND
R43, R44	2k	RES_0805	2	Yageo	Digi-Key	311-2.00KCRTR-ND
R45	100	RES_2512	1	Stackpole	Digi-Key	RMCF2512FT100RCT-ND
R46	2.21k	RES_0805	1	Yageo	Digi-Key	311-2.21KCRTR-ND
U17		SOT23-8	1	Maxim	Digi-Key	**MAX4413EKA+TCT-ND**
U18		PE-680xx	1	Pulse	Avnet	E2009QNLT
Y2	10 MHz	HC-49US	1	ECS	Digi-Key	X1080-ND

8.2 GA144 Signal map

These tables identify header pins or holes at which each chip's signals may be found.

8.2.1 Host Chip

Type	Name	Pin	Access	Description
SRAM Data Bus	d00	1	D00	Bits 0 through 17 of node 007 UP port. General purpose bidirectional parallel bus. Bits 0 through 15 are connected to the SRAM BGA and probe access is not supported except for bit 0 to probe timing. Mapping to SRAM data lines is randomized for best layout. Bits 16 and 17 are pulled down so that they will read as zero.
	d01	2	None	
	d02	3		
	d03	8		
	d04	9		
	d05	10		
	d06	11		
	d07	12		
	d08	13		
	d09	16		
	d10	21		
	d11	22		
	d12	23		
	d13	24		
	d14	25		
	d15	30		
	d16	31	R14	
	d17	32	R13	
GPIO	008.17	33	None	General purpose 4-pin node used for SRAM control (1,3) and high order address lines (5,17). Pins 1 and 3 are pulled up so that the SRAM is made inactive when chip is reset.
	008.5	34		
	008.3	35	WE-	
	008.1	36	CE-	
SRAM Address Bus	a17	37	None	Bits 17 through 0 of node 009 UP port. General purpose bidirectional parallel bus. Bits 0 through 17 are connected to the SRAM BGA and probe access is not supported except for bit 0 to probe timing. Mapping to the low order 17 SRAM address lines is randomized for best layout. A17 must be mapped directly so that the layout will accommodate chips with 128k or fewer words.
	a16	38		
	a15	39		
	a14	42		
	a13	43		
	a12	44		
	a11	45		
	a10	46		
	a09	53		
	a08	54		
	a07	55		
	a06	56		
	a05	57		
	a04	58		
	a03	65		
	a02	66		
	a01	67		
	a00	68	A00	

SERDES	001.17	27	J75	Node 001 Clock	Available at dedicated SMA connector hole patterns..
	001.1	26	J74	Node 001 Data	
SERDES	701.17	86	S17	Node 701 Clock	Connected to Target node 001 SERDES. Both chips reset to SDERDES boot.
	701.1	87	S1	Node 701 Data	
GPIO	300.17	14	J35.1	Sync clock	General purpose 2-pin node. ROM supports synchronous boot. May be connected to Target node 300.
	300.1	15	J34.1	Sync data	
GPIO	708.17	78	J23.2	Rx Input	General purpose 2-pin node. ROM supports asynchronous boot. May be connected to USB port A for IDE operations.
	708.1	79	J23.4	Tx Out	
GPIO	705.17	85	DI	Data In	General purpose 4-pin node. Normally used for boot and/or read/write on SPI Flash and/or mass storage such as MMC depending on jumpers. May also be free for application use. When MMC selected, SS- and other signals are on J40.
	705.5	84	DO	Data Out	
	705.3	81	SS-	Chip Enable-	
	705.1	80	SCK	Clock	
GPIO	100.17	20	J23.8	1-pin GPIO nodes. May be connected to USB port B for use with high level Virtual Machines.	
	200.17	18	J23.6		
	500.17	7	J22.1	1-pin GPIO node. May be used to reset the Target chip.	
	600.17	6	J39.1	1-pin GPIO node. May be used in selecting expanded SPI bus.	
	317.17	52	J21.5	1-pin GPIO nodes. Available for application use.	
	417.17	59	J21.4		
Analog In	709.ai	76	J27.3	Analog nodes whose I/O is powered by separate V_{DD}A bus. Available for application use.	
Analog Out	709.ao	77	J27.2		
Analog In	713.ai	73	J27.4		
Analog Out	713.ao	72	J27.5		
Analog In	717.ai	69	J27.8		
Analog Out	717.ao	70	J27.7		
GPIO	715.17	71	J27.6	General purpose 1-pin node whose pin is shared (read only) by the above analog nodes and may be used by them for timing or other purposes.	
Analog In	617.ai	61	J21.2	Analog node whose I/O is powered by V_{DD}I bus.	
Analog Out	617.ao	63	J21.1		
GPIO	517.17	60	J21.3	General purpose 1-pin node whose pin is shared (read only) by Analog 617.	
Analog In	117.ai	48	J21.8	Analog node whose I/O is powered by V_{DD}I bus.	
Analog Out	117.ao	50	J21.7		
GPIO	217.17	51	J21.6	General purpose 1-pin node whose pin is shared (read only) by Analog 117.	
Input	RESET-	88	J20.1	Reset signal, active low. Also pin J20.2.	
Power	V_{DD}C	5	J10.2	Core power bus. Powers F18A computers, and parts of I/O circuitry (such as registers) that are internal to them.	
		17			
		29			
		41			
		49			
		62			
		75			
		83			
Power	V_{DD}I	4	J11.2	I/O power bus. Powers I/O pads including the parts of the I/O circuitry collocated with the pads. Includes analog pads for nodes 117 and 617.	
		19			
		28			
		40			
		47			
		64			
		82			
Power	V_{DD}A	74	J11.2	Analog power bus for pads of nodes 709, 713 and 717.	
Ground	GND	DAP	any gnd	Common ground and heat sink.	

8.2.2 Target Chip

Type	Name	Pin	Access	Description	
Bus I/O	d00	1	J30.1	Bits 0 through 17 of node 007 UP port. General purpose bidirectional parallel bus, such as external memory data.	
	d01	2	J30.2		
	d02	3	J30.3		
	d03	8	J30.6		
	d04	9	J30.7		
	d05	10	J30.8		
	d06	11	J30.9		
	d07	12	J30.10		
	d08	13	J30.11		
	d09	16	J30.12		
	d10	21	J30.15		
	d11	22	J30.16		
	d12	23	J31.1		
	d13	24	J31.2		
	d14	25	J31.3		
	d15	30	J31.4		
	d16	31	J31.5		
	d17	32	J31.6		
GPIO	008.17	33	J31.7	General purpose 4-pin node. Might be used for memory or bus control and handshake lines.	
	008.5	34	J31.8		
	008.3	35	J31.9		
	008.1	36	J31.10		
Bus I/O	a17	37	J31.11	Bits 17 through 0 of node 009 UP port. General purpose bidirectional parallel bus, such as external memory address.	
	a16	38	J31.12		
	a15	39	J31.13		
	a14	42	J31.14		
	a13	43	J31.15		
	a12	44	J31.16		
	a11	45	J36.15		
	a10	46	J36.14		
	a09	53	J36.9		
	a08	54	J36.8		
	a07	55	J36.7		
	a06	56	J36.6		
	a05	57	J36.5		
	a04	58	J36.4		
	a03	65	J32.15		
	a02	66	J32.14		
	a01	67	J32.13		
	a00	68	J32.12		
SERDES	001.17	27	S17	Node 001 Clock	Connected to Host node 701 SERDES. Both chips reset to SDERDES boot.
	001.1	26	S1	Node 001 Data	
SERDES	701.17	86	J28.2	Node 701 Clock	Available for experimentation.
	701.1	87	J28.4	Node 701 Data	
GPIO	300.17	14	J35.2	Sync clock	General purpose 2-pin node. ROM supports synchronous boot. May be connected to Host node 300.
	300.1	15	J34.2	Sync data	

GPIO	708.17	78	J23.10	Rx Input	General purpose 2-pin node. ROM supports asynchronous boot. May be connected to USB port C for IDE operations.
	708.1	79	J23.12	Tx Out	
GPIO	705.17	85	J32.1	Data In	General purpose 4-pin node. If 705.17 is low on reset, ROM will attempt SPI memory boot using signal assignments shown, driving signals on 705.5, 3, 1, and will leave these in output mode unless programmed otherwise.
	705.5	84	J32.2	Data Out	
	705.3	81	J32.3	Chip Enable-	
	705.1	80	J32.4	Clock	
GPIO	100.17	20	J30.14	General purpose 1-pin nodes. No special ROM or interconnections.	
	200.17	18	J30.13		
	500.17	7	J30.5		
	600.17	6	J30.4		
	317.17	52	J36.10		
	417.17	59	J36.3		
Analog In	709.ai	76	J32.6	Analog nodes whose I/O is powered by separate V_{DD}A bus.	
Analog Out	709.ao	77	J32.5		
Analog In	713.ai	73	J32.7		
Analog Out	713.ao	72	J32.8		
Analog In	717.ai	69	J32.11		
Analog Out	717.ao	70	J32.10		
GPIO	715.17	71	J32.9	General purpose 1-pin node whose pin is shared (read only) by the above analog nodes and may be used by them for timing or other purposes.	
Analog In	617.ai	61	J36.1	Analog node whose I/O is powered by V_{DD}I bus.	
Analog Out	617.ao	63	J32.16		
GPIO	517.17	60	J36.2	General purpose 1-pin node whose pin is shared (read only) by Analog 617.	
Analog In	117.ai	48	J36.13	Analog node whose I/O is powered by V_{DD}I bus.	
Analog Out	117.ao	50	J36.12		
GPIO	217.17	51	J36.11	General purpose 1-pin node whose pin is shared (read only) by Analog 117.	
Input	RESET-	88	J22.2	Reset signal, active low. Also pins J22.4 and 6.	
Power	V_{DD}C	5	J14.2	Core power bus. Powers F18A computers, and parts of I/O circuitry (such as registers) that are internal to them.	
		17			
		29			
		41			
		49			
		62			
		75			
		83			
Power	V_{DD}I	4	J15.2	I/O power bus. Powers I/O pads including the parts of the I/O circuitry collocated with the pads. Includes analog pads for nodes 117 and 617.	
		19			
		28			
		40			
		47			
		64			
		82			
Power	V_{DD}A	74	J16.2	Analog power bus for pads of nodes 709, 713 and 717.	
Ground	GND	DAP	any gnd	Common ground and heat sink.	

8.3 Connector Pinouts

8.3.1 Power Control Section

External Connector

Pin 1 of J1 is oriented toward the bottom edge of the board and thus is an exception to the rule.

J1

10	Gnd
9	User supply, J4
8	Gnd
7	User supply, J5
6	Gnd
5	User supply, J6
4	Gnd
3	External Host Pwr
2	Gnd
1	External Target Pwr

Single Pins

J4	User supply, J1.9
J5	User supply, J1.7
J6	User supply, J1.5

Host Power Select

J10

1	External Host Pwr
2	V_{DD}C to Host
3	Main 1.8v Bus

J11

1	External Host Pwr
2	V_{DD}I and A to Host
3	Main 1.8v Bus

Target Power Select

J14

1	External Target Pwr
2	V_{DD}C to Target
3	Main 1.8v Bus

J15

1	External Target Pwr
2	V_{DD}I to Target
3	Main 1.8v Bus

J16

1	External Target Pwr
2	V_{DD}A to Target
3	Main 1.8v Bus

8.3.2 USB Serial Interfaces

Port Data Connections to Host and Target

J23

Incoming from Port A	1	2	Host 708.17
Outgoing to Port A	3	4	Host 708.1
Incoming from Port B	5	6	Host 200.17
Outgoing to Port B	7	8	Host 100.17
Incoming from Port C	9	10	Target 708.17
Outgoing to Port C	11	12	Target 708.1

Port A Access

J7	FTDI 3.3v Pwr

J8

1	DTR signal
2	CBUS2
3	CBUS3
4	CBUS4

Port B Access

J12	FTDI 3.3v Pwr
J24	RTS signal

J13

1	DTR signal
2	CBUS2
3	CBUS3
4	CBUS4

Port C Access

J19	FTDI 3.3v Pwr

J17

1	DTR signal
2	CBUS2
3	CBUS3
4	CBUS4

8.3.3 Host Chip

Probe Points

CE-	SRAM chip enable from 008.1
WE-	SRAM write enable from 008.3
D00	SRAM data bit
A00	SRAM address bit
SS-	Chip select for SPI Flash chip
SCK	Clock line for SPI bus (selectively enabled to the SD socket)
DO	Data out bus from G144 to SPI devices
DI	Data in bus from SPI devices to G144

Reset and Boot

J20

Host RESET pin	1	2	Host RESET pin
USB A RTS signal	3	4	From J25.2

J25

1	Watchdog/Reset Chip
2	To J20.4
3	Host reset ckt & button.

J26 "NO-BOOT" JMPR

1	Host 705.17
2	1K Pull-up to 1.8v

WDI

1	Watchdog Input

SPI Bus Expansion

J39

1	Host 600.17
2	FLASHENABLE-
3	Ground

J37

FLASHENABLE- on SPI bus.	1	2	2 inputs to NAND. Output low enables MMC on SPI bus.
	3	4	

Additional Host I/O

Host pins	J21		*NIC Signals*
617.ao	1		
617.ai	2	J48	
517.17	3	1	Y2 xtal hi
417.17	4	2	Y2 xtal hi
317.17	5	3	Tx (to opamp)
217.17	6	4	Rx (raw)
117.ao	7		
117.ai	8		

J27

1	Ground
2	709.ao
3	709.ai
4	713.ai
5	713.ao
6	715.17
7	717.ao
8	717.ai

J41 Can be 5V source

1	V_{CC}
2	V_{CC}

J76

Connect 5V here for E-NET board	1	2	Connect 5V here for onboard Ether circuit

8.3.4 Target Chip

Probe Points

S17	SERDES Clock between Host and Target
S1	SERDES Data

Reset and Host Communication

J22

Host 500.17	1	2	Target RESET- pin
USB C RTS signal	3	4	
Target reset circuit	5	6	

J35

1	Host 300.17
2	Target 300.17

J34

1	Host 300.1
2	Target 300.1

Uncommitted Target Pins

J30

d00	1	2	d01
d02	3	4	600.17
500.17	5	6	d03
d04	7	8	d05
d06	9	10	d07
d08	11	12	d09
200.17	13	14	100.17
d10	15	16	d11

J31

d12	1	2	d13
d14	3	4	d15
d16	5	6	d17
008.17	7	8	008.5
008.3	9	10	008.1
a17	11	12	a16
a15	13	14	a14
a13	15	16	a12

J32

705.17	1	2	705.5
705.3	3	4	705.1
709.ao	5	6	709.ai
713.ai	7	8	713.ao
715.17	9	10	717.ao
717.ai	11	12	a00
a01	13	14	a02
a03	15	16	617.ao

J36

617.ai	1	2	517.17
417.17	3	4	a04
a05	5	6	a06
a07	7	8	a08
a09	9	10	317.17
217.17	11	12	117.ao
117.ai	13	14	a10
a11	15	16	Ground

J28

Ground	1	2	701.17 SERDES clock
	3	4	701.1 SERDES data

8.3.5 Prototyping Area

SD/MMC Socket Signals

SD Socket signals	J38	J40	*SPI Bus signals*
CLK/SCLK	1	1	SPI CLK MMC
DAT3/CS-	2	2	SPI CS- MMC
CMD/SI	3	3	SPI DO
DAT0/SO	4	4	SPI DI
V_{DD}	5	5	1.8v

J33	*SD Socket Signals*
1	DAT1
2	DAT2
3	Card Present
4	Write Protect

TI TXB0108 Level Shifterss

Each level shifter is surrounded by this hole pattern:

A2	V_{CC}A	A1	B1	V_{CC}B	B2
A3					B3
A4					B4
A5					B5
A6					B6
A7	A8	OE	V_{SS}	B8	B7

Convenience Logic

TP4	NAND 1 Input
TP5	NAND 1 Input
TP11	NAND 1 Output
TP6	NAND 2 Input
TP7	NAND 2 Input
TP12	NAND 2 Output
TP8	NAND 3 Input
TP9	NAND 3 Input
TP13	NAND 3 Output
TP2	OR Input
TP3	OR Input
TP10	OR Output

DB9 RS232 site Left (J52)

J54

1	RX Incoming
2	TX Outgoing
3	RTS Incoming

Note these signals are on chip side of minimal quasi-RS232 transceiver.

General Purpose LEDs

J57

1	V_{DD} for D12
2	V_{DD} for D13
3	V_{DD} for D14
4	V_{DD} for D15

DB9 RS232 site Right (J58)

J59

1	RX Incoming
2	TX Outgoing
3	RTS Incoming

Note these signals are on chip side of minimal quasi-RS232 transceiver.

VGA site (J70)

J67

1	RED
2	GREEN
3	BLUE
4	HSYNC
5	VSYNC
6	gnd

USB site (J71)

J68

1	V_{CC}
2	D+
3	D-

RJ48 site (J69)

J66

1	TX+
2	TX-
3	RX+
4	RX-
5	n/c

Audio site (J62, 63, 64)

J65

1	RING
2	NC TIP SWITCH
3	TIP
4	SLEEVE

J60

1	RING
2	NC TIP SWITCH
3	TIP
4	SLEEVE

J61

1	RING
2	NC TIP SWITCH
3	TIP
4	SLEEVE

8.4
8.4
8.4
8.4
8.4

8.4 Errata

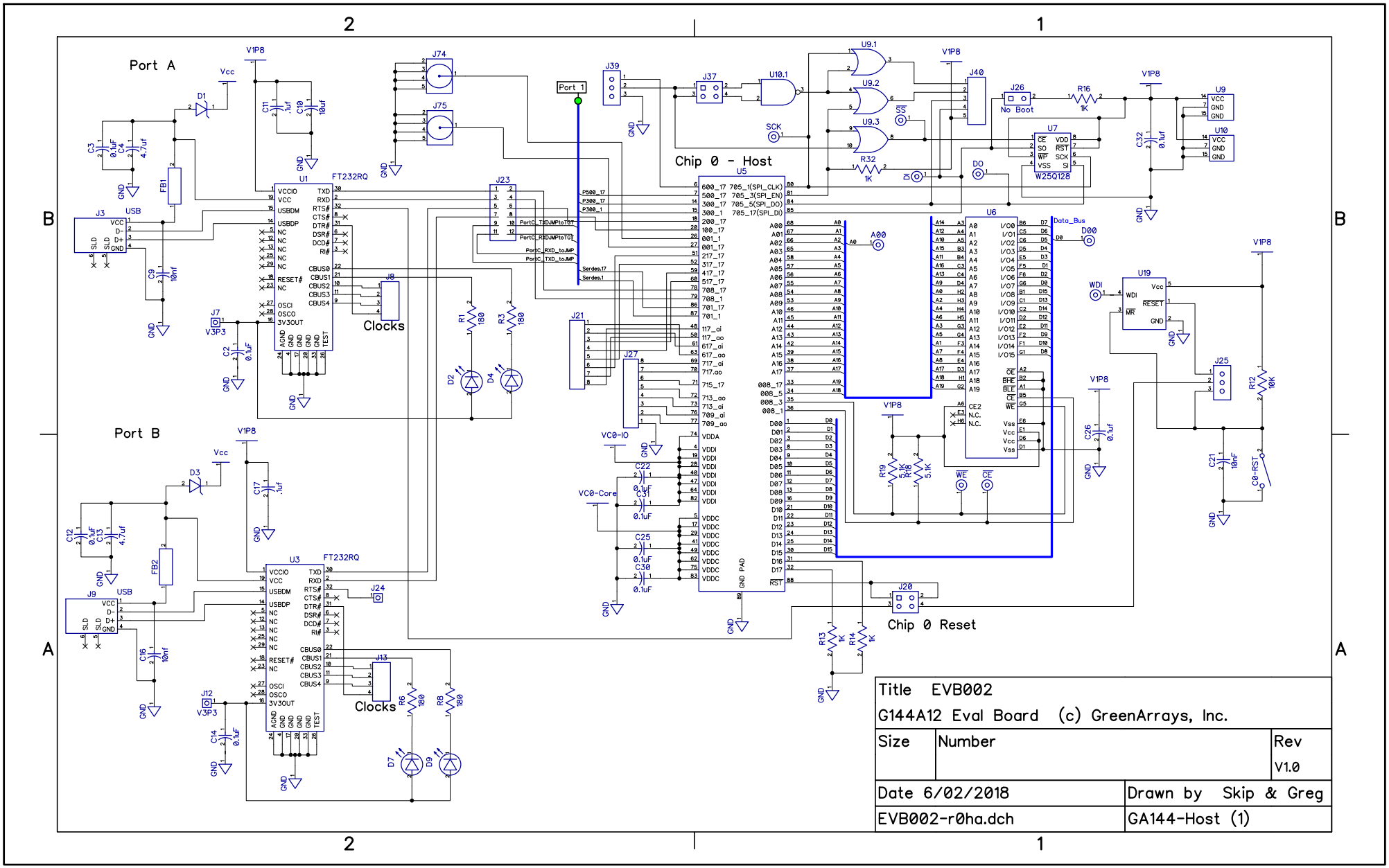
Known problems at the time of this writing are as follow:

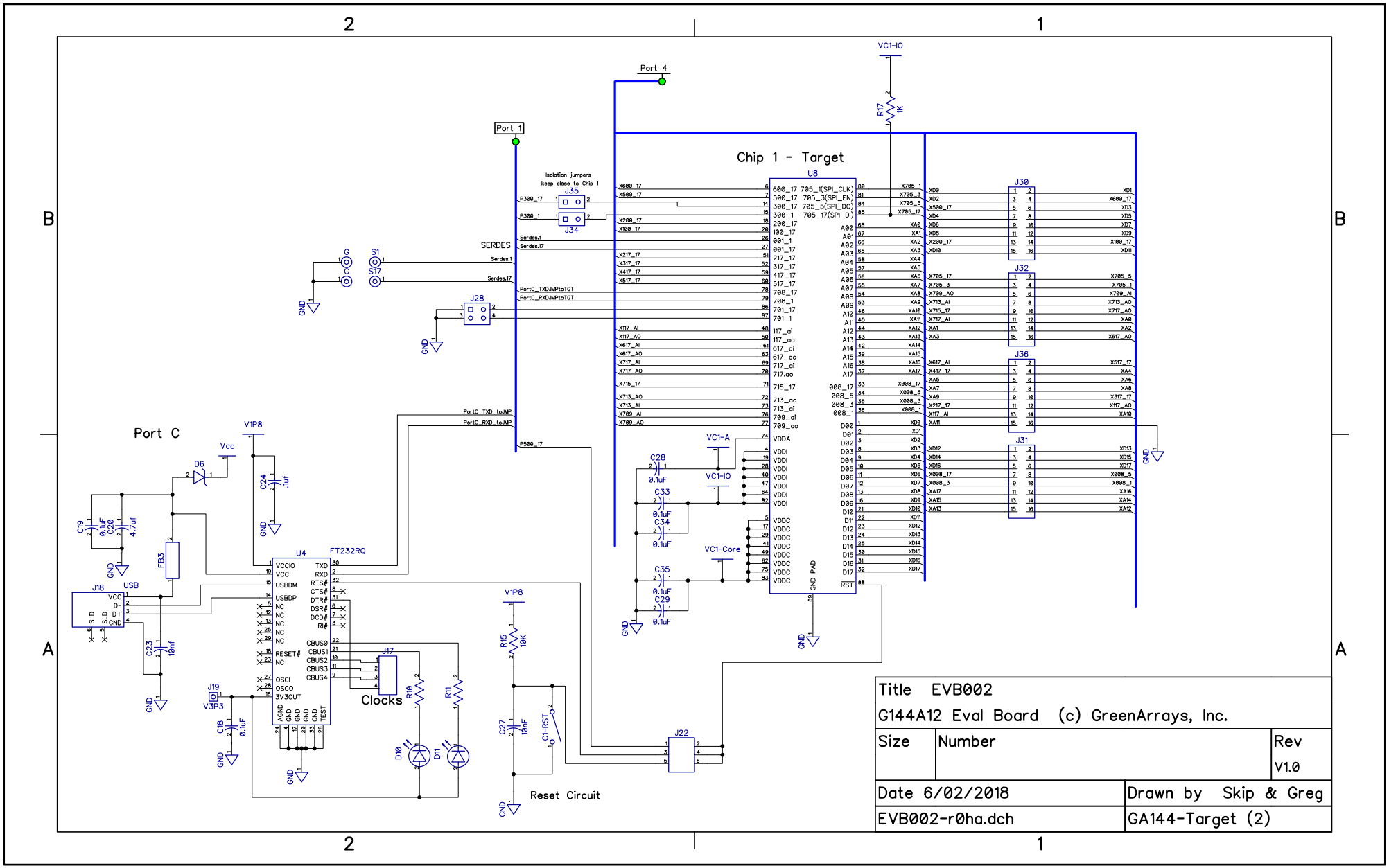
PCB REV	DESCRIPTION	FIX OR WORK-AROUND

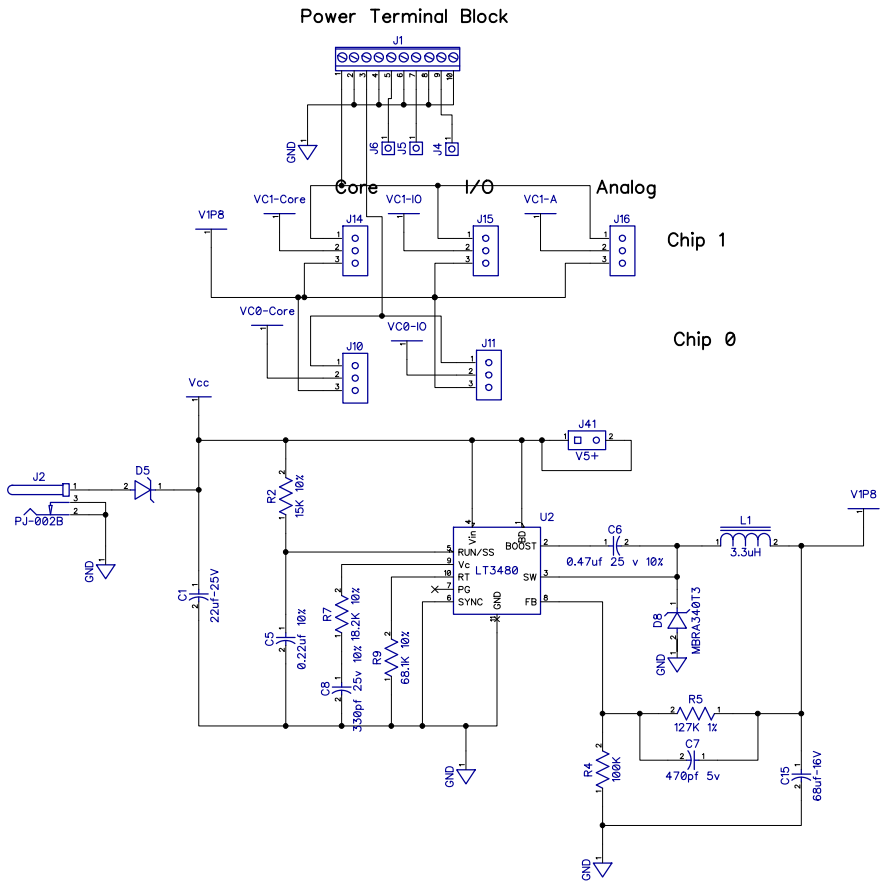
8.5 Schematics and Layout

The following eleven pages may be used to print or view high resolution renderings of these graphics.

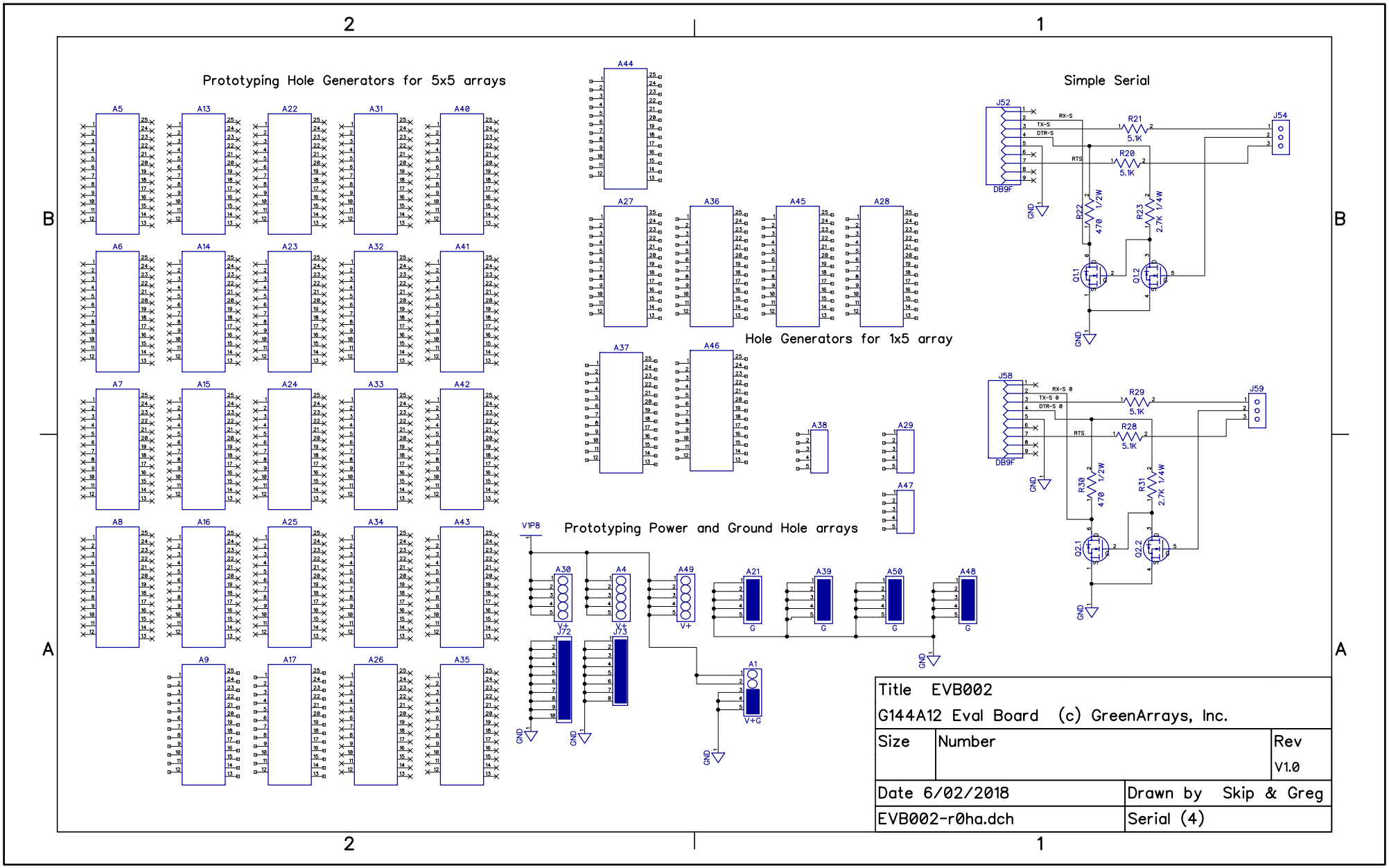
Status of artwork: These are production drawings.

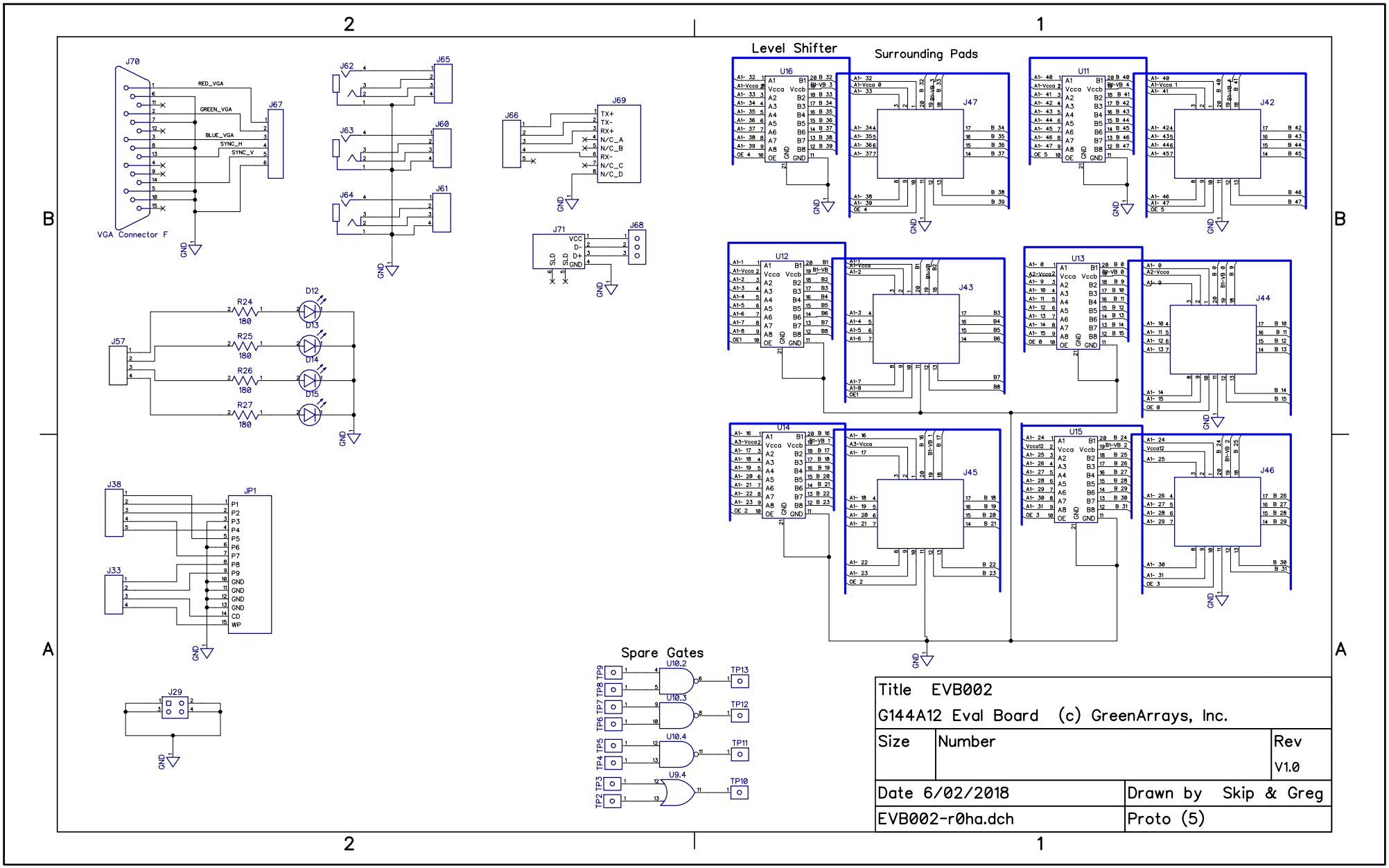

Port A
Port B
Chip 0 - Host
Chip 0 Reset
Clocks
Clocks
No Boot
Port 1
Data_Bus
Title EVB002
G144A12 Eval Board (c) GreenArrays, Inc.
Size
Number
Rev
V1.0
Date 6/02/2018
Drawn by Skip & Greg
EVB002-r0ha.dch
GA144-Host (1)

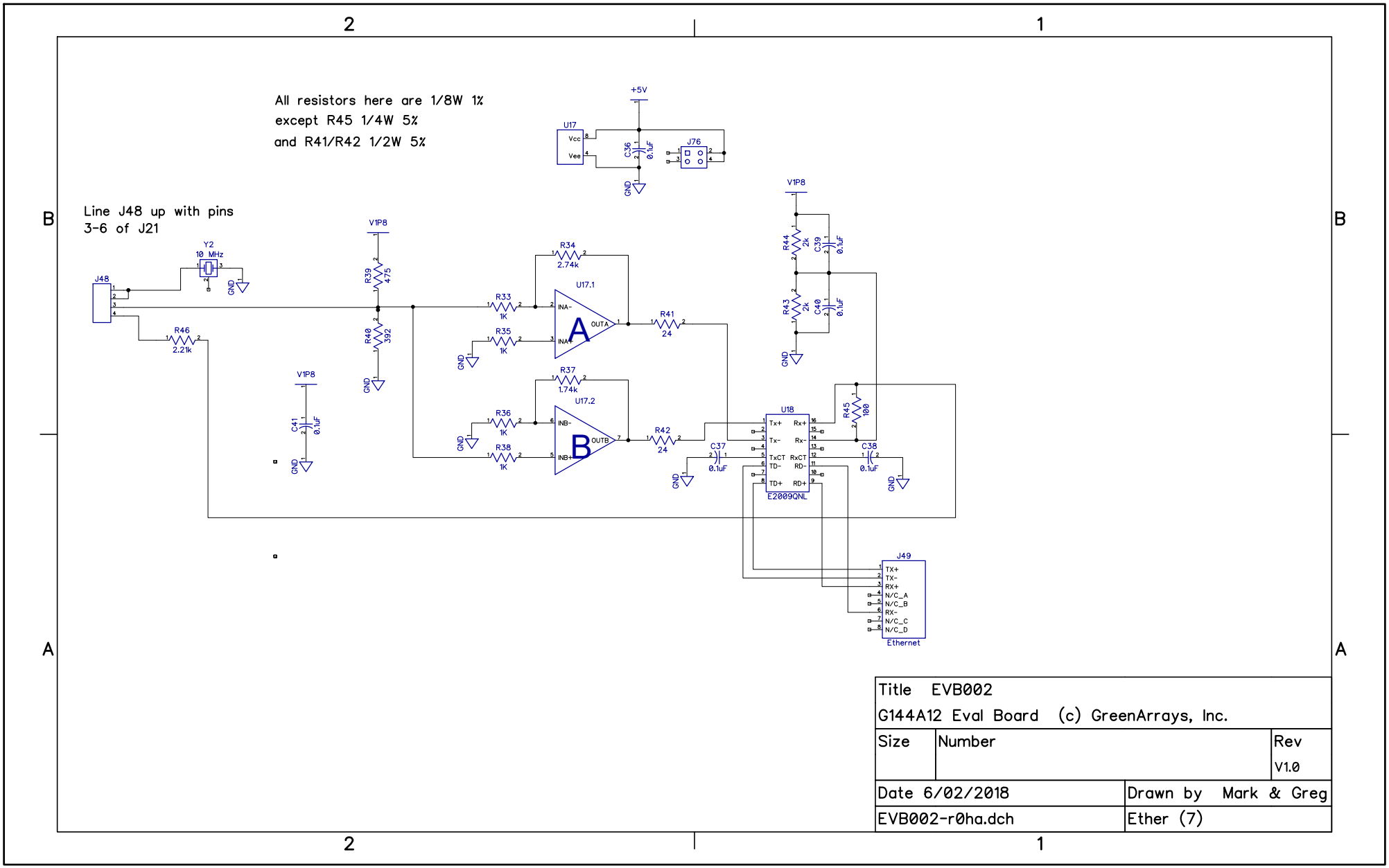

Chip 1 - Target
U8
Port 1
Port 4
Isolation jumpers
keep close to Chip 1
J35
J34
SERDES
S1
S17
J28
Port C
U4
FT232RQ
USB
J18
J19
V3P3
J17
Clocks
J22
Reset Circuit
J30
J32
J36
J31
VC1-IO
VC1-A
VC1-Core
V1P8
Vcc
R17
1K
R15
10K
R10
R11
C1-RST
D6
D10
D11
FB3
C19
C20
C24
C23
C18
C27
C28
C33
C34
C35
C29
0.1uF
4.7uf
.1uf
10nf
GND
Title EVB002
G144A12 Eval Board (c) GreenArrays, Inc.
Size
Number
Rev
V1.0
Date 6/02/2018
Drawn by Skip & Greg
EVB002-r0ha.dch
GA144-Target (2)



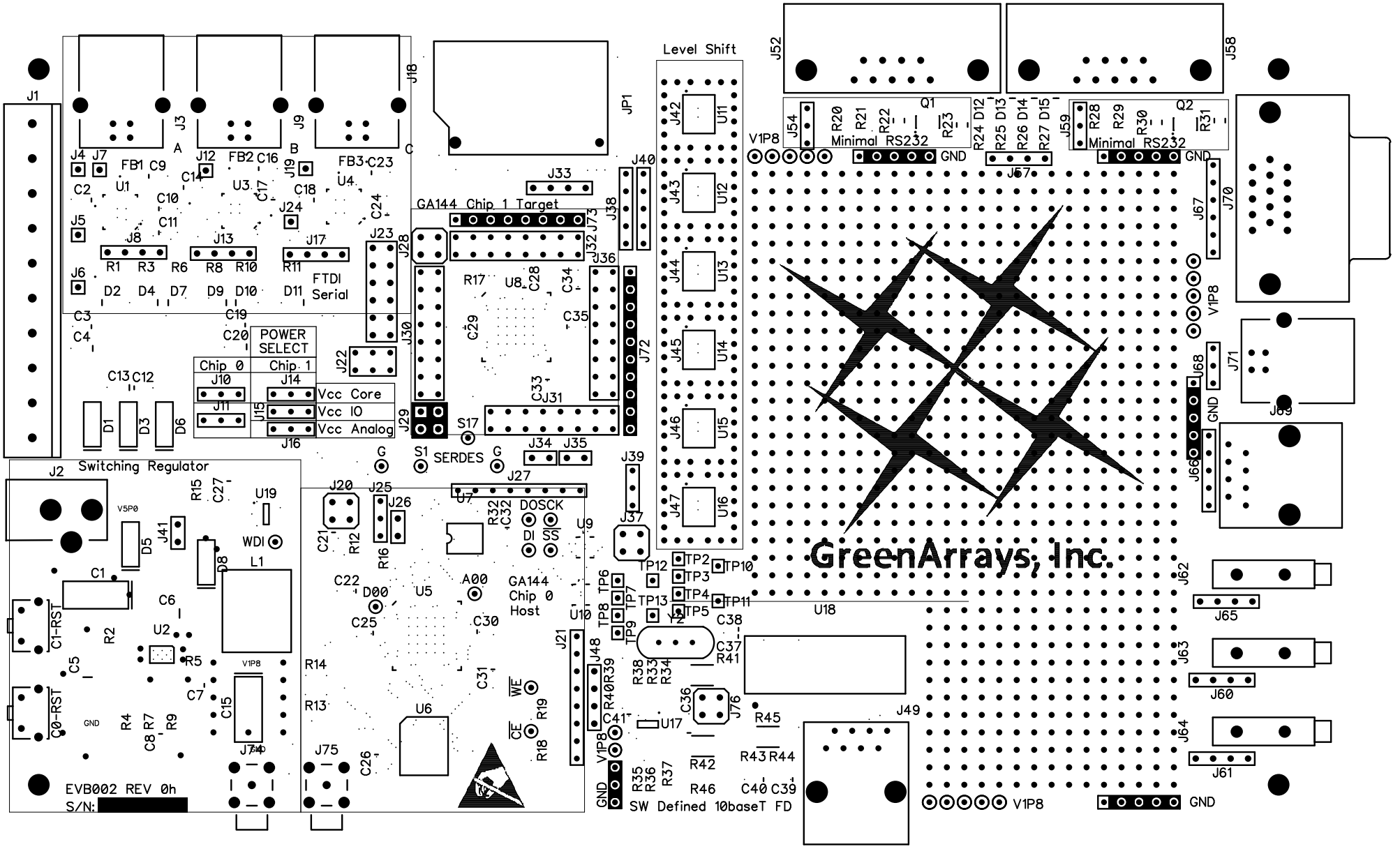
Title EVB002		
G144A12 Eval Board (c) GreenArrays, Inc.		
Size	Number	Rev V1.0
Date 6/02/2018	Drawn by Skip & Greg	
EVB002-r0ha.dch	Supply (3)	


Prototyping Hole Generators for 5x5 arrays
Hole Generators for 1x5 array
Prototyping Power and Ground Hole arrays
Simple Serial
Title EVB002
G144A12 Eval Board (c) GreenArrays, Inc.
Size
Number
Rev
V1.0
Date 6/02/2018
Drawn by Skip & Greg
EVB002-r0ha.dch
Serial (4)

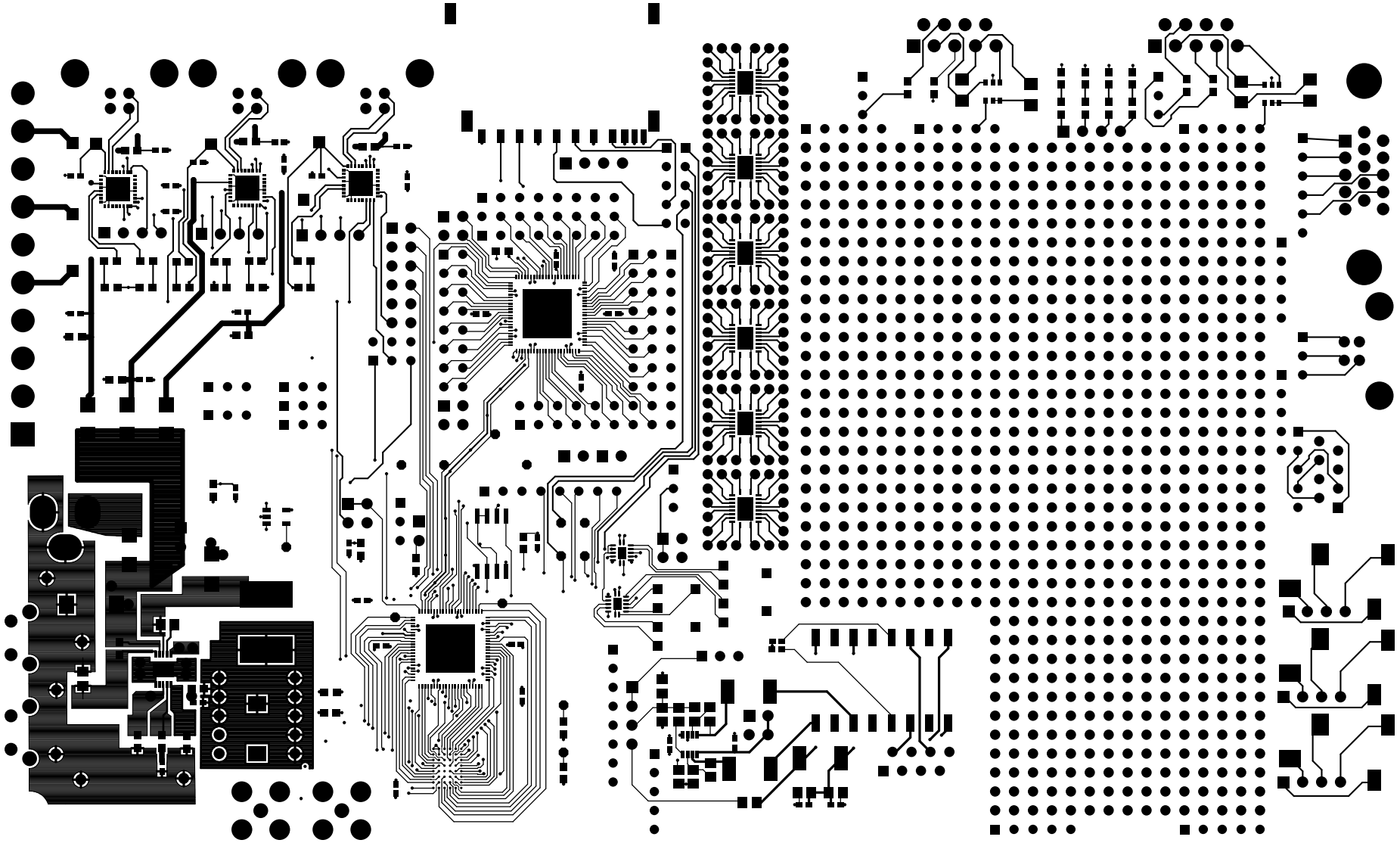

Level Shifter
Surrounding Pads
VGA Connector F
RED_VGA
GREEN_VGA
BLUE_VGA
SYNC_H
SYNC_V
Spare Gates
Title EVB002
G144A12 Eval Board (c) GreenArrays, Inc.
Size
Number
Rev
V1.0
Date 6/02/2018
Drawn by Skip & Greg
EVB002-r0ha.dch
Proto (5)



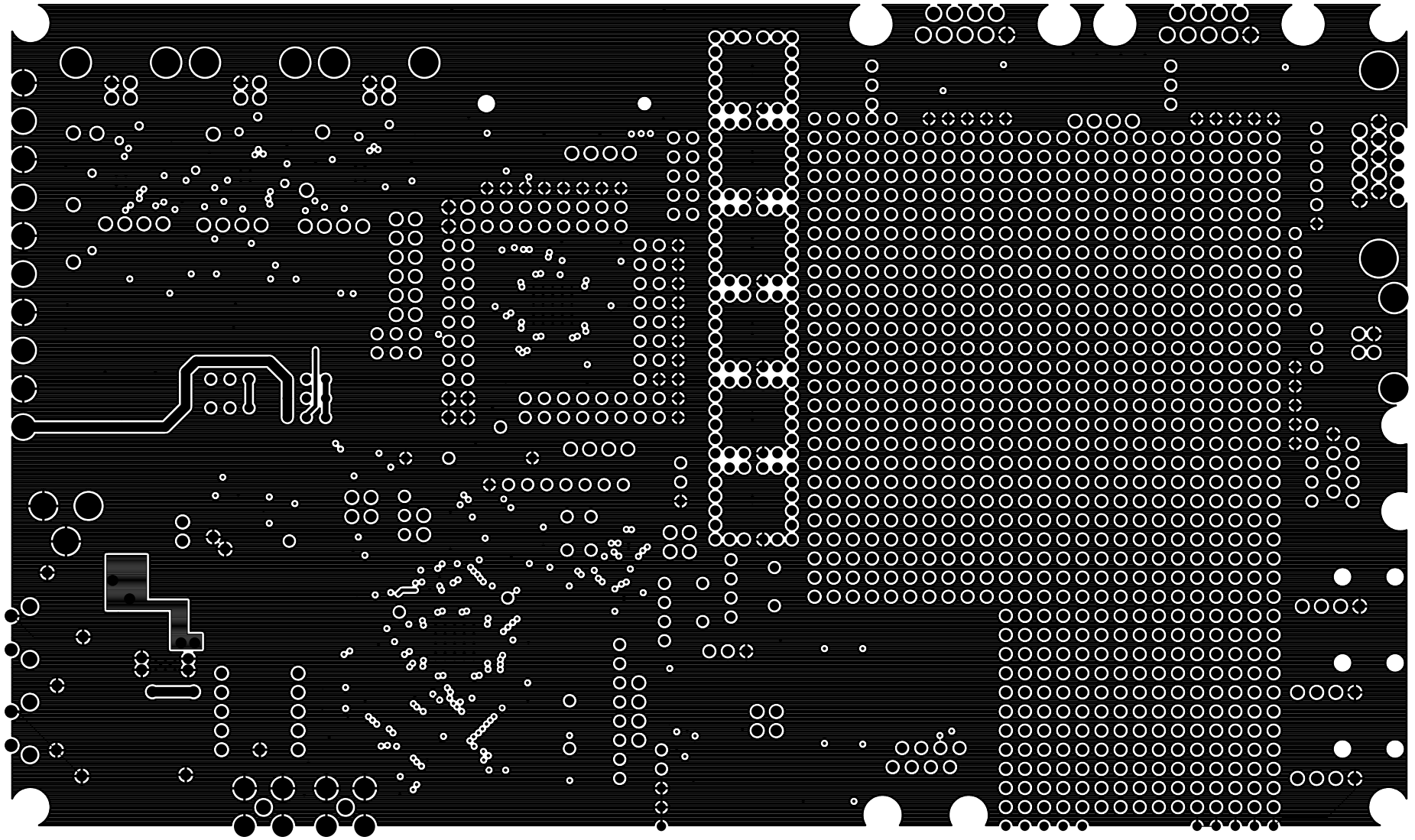
Title EVB002		
G144A12 Eval Board (c) GreenArrays, Inc.		
Size	Number	Rev V1.0
Date 6/02/2018	Drawn by Mark & Greg	
EVB002-r0ha.dch	Ether (7)	


Level Shift
GA144 Chip 1 Target
FTDI Serial
POWER SELECT
Chip 0
Chip 1
Vcc Core
Vcc IO
Vcc Analog
Switching Regulator
SERDES
DOSCK
GA144 Chip 0 Host
Minimal RS232
Minimal RS232
GreenArrays, Inc.
EVB002 REV 0h
S/N:
SW Defined 10baseT FD

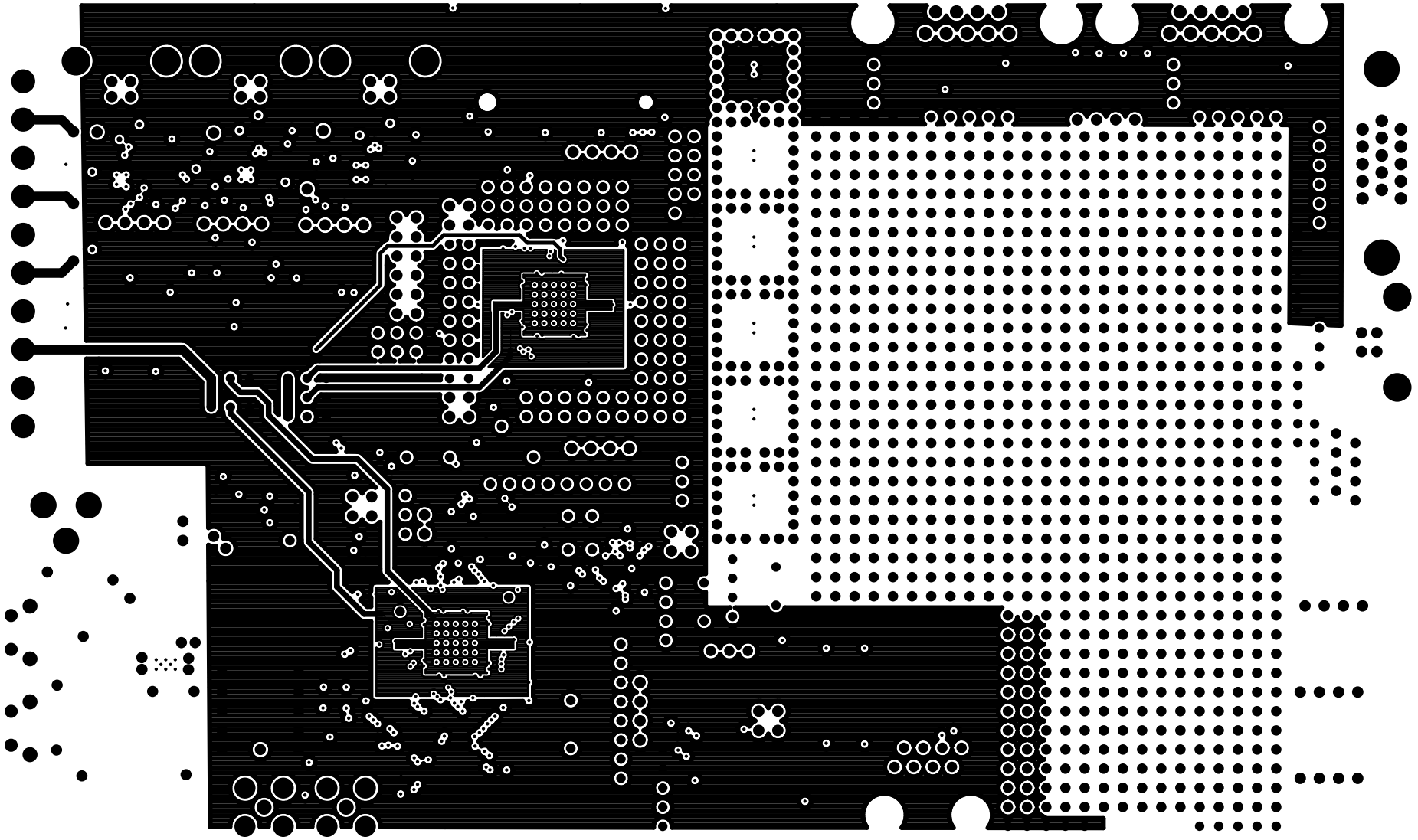
New_job.bin L11: Top.gbr (SIG)



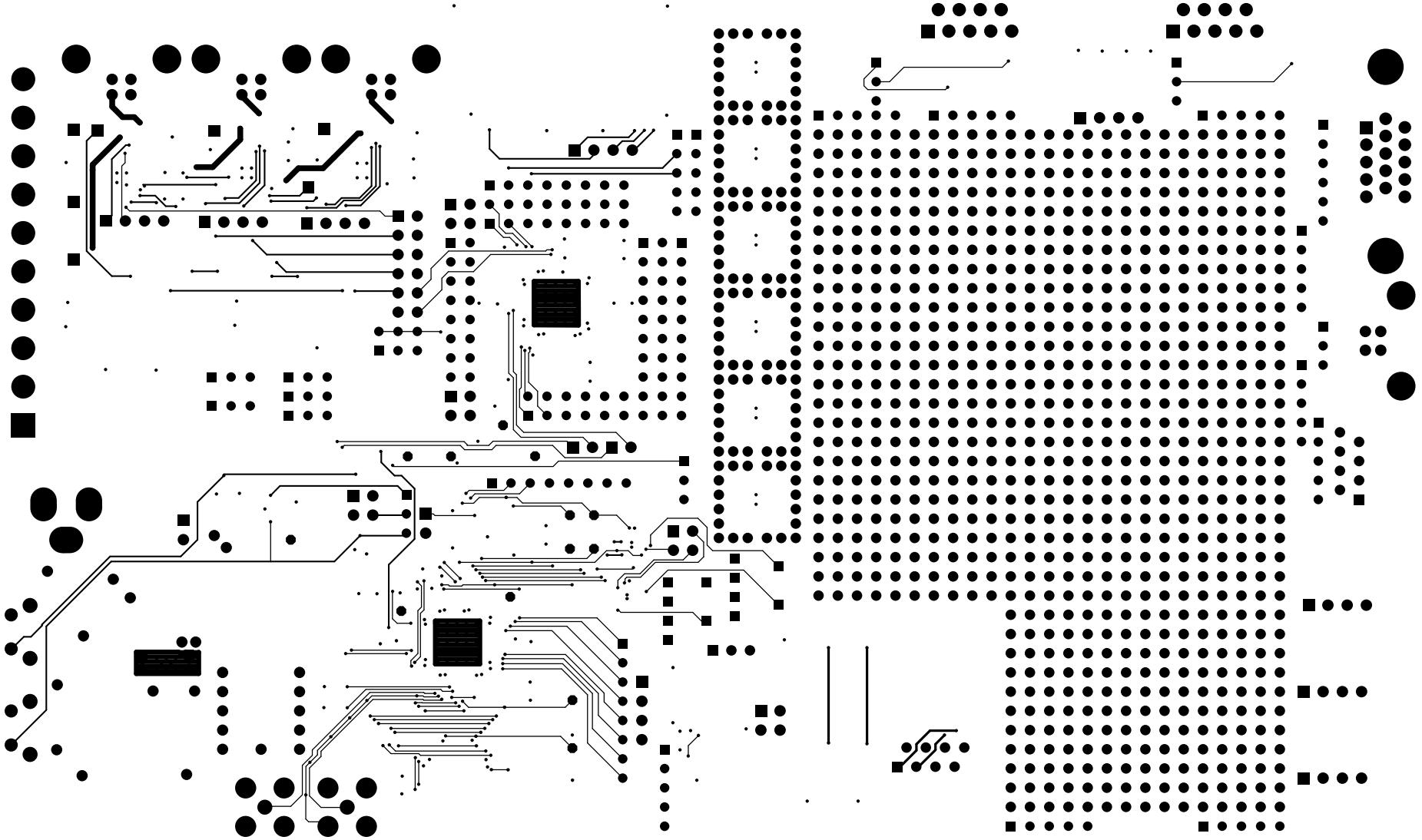
New_job.bin L9: GND.gbr (SIG)



New_job.bin L17: VCC.gbr (SIG)



New_job.bin L3: Bottom.gbr (SIG)



9. Data Book Revision History

REVISION	DESCRIPTION
180415	Convert from EVB001 to EVB002.
190506	Preliminary for pre-release of EVB002.
190520	Initial release of EVB002.

GreenArrays®

Product Data Book DB014 *Revised 5/20/19*

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