Actual size

1cm x 1cm

Isolated-Linear Processor

A robust multicomputer

FEATURES

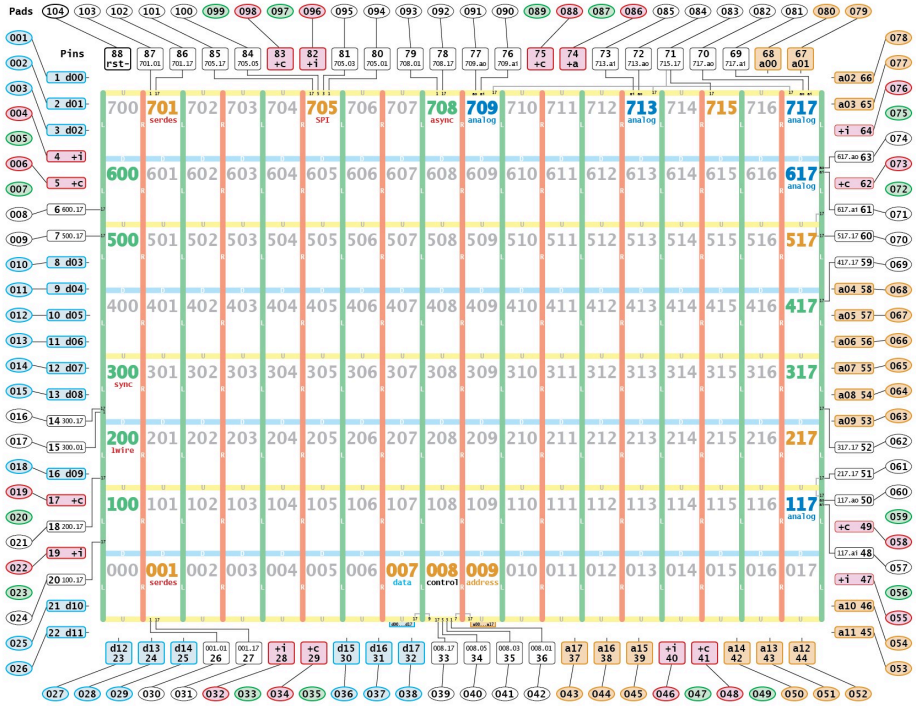
- 144 independent-modular computers
- Suitable for 4-layer PCBs like *Volatco*
- Up to 96 billion operations per second
- Instantaneous power ranges from 14 microwatts to 650 milliwatts.
- Energy consumed depends on each computer's duty cycle, controlled by software and events, with granularity in picoseconds
- Negligible time and energy expended starting and stopping each node
- Suspended nodes respond to internal events in picoseconds and external events in nanoseconds
- High impedance (<3pF, >200MΩ) inputs
- Five analog inputs and five outputs
- Two 18-bit parallel interfaces
- 25 programmable digital I/O pins
- Overall digital I/O bandwidth can exceed three gigabits per-second with software-based bit parsing and an additional 800 megabits per-second when both SERDES are operating
- Bootable via SPI or any of four serial protocols; custom ROM available
- 9216 words RAM and same amount of ROM distributed among all nodes—equivalent to 41472 total bytes
- Minimal external components needed to build a newly-designed system

APPLICATIONS

- Machine intelligence, Bayesian networks
- Ideal reinforcement learning
- Energy harvesting applications
- Robotics and autonomous devices
- Remote sensing and data reduction
- Homeostatic dynamic control for parallel-pipelined modes
- Image processing
- Cryptography
- High-power systems signal processing
- Simulation and synthesis
- Workload synchronization
- Lower computational energy per unit
- A native internal systems development architecture

OVERVIEW

An extraordinarily powerful and versatile computing chip that consists of an 18x8 array of architecturally-identical, independent and fully-described computers, or *nodes*, each of which operates asynchronously. Each is capable of performing a basic ALU instruction in ~1.5 nanoseconds for an energy cost of 7 picojoules. Nothing else available compares to this technology. Twenty-two of the computers at the edges of the array have one or more I/O pins and one of several classes of circuitry associated with them to improve multi-tasking versatility, as illustrated in the following figure.



Nodes numbered in green have one or two GPIO pins; those in blue have analog I/O; those in orange have a digital I/O with specialized purposes: Nodes 001 and 701 have high-speed SERDES; node 705 has four pins useable as an SPI bus; nodes 217, 517, and 715 have a GPIO pin whose read-line is connected to one or more analog nodes for sample synchronization. Nodes 007, 008, and 009 in-combination control two 18-bit parallel buses and four GPIO pins that are used to control external memory for the most commonly-integrated solutions widely-available to GPUs. These and the SPI bus are available for other uses where required by the application environment.

All nodes are suspended after reset and are prepared to execute instructions coming from any neighbor node via a communications port. Six of these are also waiting for external signals, which is interpreted as boot frames. Node 001 and 701 SERDES will execute instructions received; node 200 has ROM for high-speed 1-wire protocol, node 300 listens for 2-wire synchronous, node 708 for RS-232 framed asynchronous, and node 705 bootable from a SPI flash memory device.

When rapid product requirements for responsiveness, computing power and energy, and robust control are paramount, this processor is the ideal compute for rapid product and infrastructure development. We support custom configuration for tight integration of customers' needs through our **Application Discovery Program**. Send us a query.

Isolated-Linear Processor

Extreme async at your fingertips

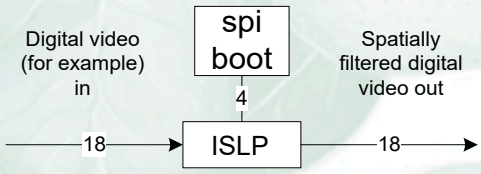
SUITABILITY: The ISLP is designed to support the largest and most demanding computing challenges that can be addressed with a modest-sized die in a relatively inexpensive and easy-to-use package while still using well less than 650mW in most practical applications. The geometry allows for ubiquitous numbers of parallel paths and/or pipeline stages, or for complex flowgraphs in control, simulation, or DSP applications. Clusters of nodes devoted to functions such as deep cryptographic algorithms are easily placed, and the cluster needed to control external memory and run a high-level language from it is well out of the way, with good surface area for interaction with other functions. It is ideal as a universal prototyping platform for applications required to run in such a small package.

SOFTWARE SUPPORT: A complete software development platform is available, which includes a compiler for machine code, an interactive simulator, and an interactive development and debugging environment (IDDE). Complete source code is provided so that all components of this platform are extensible for any application scenario in any kind of control environment.

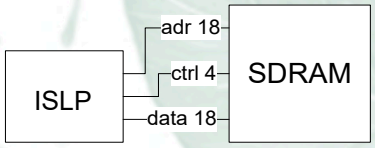
When complex programs are required, the ISLP supports polyForth®, Lua, and Lisp running from external SRAM or SDRAM. Typically, three to five nodes control the external memory and two nodes interpret the high-level language itself.

PACKAGE: The ISLP is available in a 10x10mm, 88-pin QFN with 0.4mm pin pitch. All ground connections are made to the central die-attach paddle. Operational range is between –40C and 125C and is suitable for radiation-intensive environments.

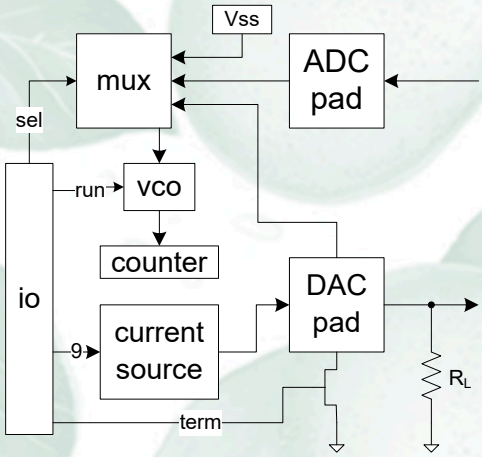
Sym	Description	Min	Typ	Max	Units	Test Condition
Cpin	I/O pin capacitance with Vdd = 0V		2.8		pF	I/O to Vss
ILI	Input leakage current (tristate)	2.4	3.5	5.5	nA	Vin to Vdd or Vss
IR	Effective input resistance (tristate)		320		MΩ	
ILpd	Weak pulldown current (in saturation)	30	36	43	µA	Vin to Vdd
VIH	Input high level		1.1		V	Note: No hysteresis
VIL	Input low level		0.650		V	
ISH	Max current sourced (in saturation)	36	42	49	mA	Vout to Vss
ISL	Max current sunk (in saturation)	36	40	44	mA	Vout to Vdd
ROH	Output source res. for 0.5 Vdd @ Vout		23.5	25.1	Ω	Vout to Vss
ROL	Output sink res. for 0.5 Vdd @ Vout		21.5		Ω	Vout to Vdd
ICC	Core current, all nodes running	468	540	612	mA	Vdd to VddC
ICCs	Core current, all nodes suspended	2	7	31	µA	
ICCg	Core current per running computer	3.25	3.75	4.25	mA	
ICCgs	Core current per suspended computer	15	50	210	nA	
Vdd	Supply voltage	1.62	1.8	2.0	V	Below @ these Vdd
Voh	Output high sourcing 10 mA	1.37	1.65	1.86	V	Vout to Vss
Vol	Output low sinking 10 mA	0.122	0.125	0.270	V	Vout to Vdd



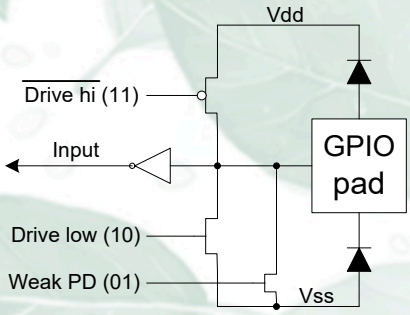
Two-chip higher-order filter



Direct control of SDRAM or SRAM without glue code



Analog I/O Peripherals



GPIO

Pin and pad capacitance ≈2.95 pF
Input leakage ≈7.5 nA (≈240 MΩ)
Short circuit source ≈23 mA, sink ≈22 mA
Weak Pulldown ≈38 µA in saturation

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